Design and Implementation of the RF Transceiver for LTE User Equipment.

Marwa Mansour Abd el-Fattah
PhD. Student in ASU

Supervision Committee

Prof. Abdelhalim Abdelnaby Zekry
Prof. Heba Ahmed Shawkey
Dr. Mohamed Kamal Abdelrahman Ali

Department of Electronics and Communication Engineering

List of publications

- Marwa Mansour, Abdelhalim Zekry, Mohammed K. Ali, and Heba Shawkey, "**A comparative study between Class-C and Class-B quadrature voltage-controlled power oscillator for multi-standard applications**", Microelectronics Journal, vol. 98 – no. 8, pp. 104726, April 2020. IF=1.564
- Marwa Mansour, Abdelhalim Zekry, Mohammed K. Ali, and Heba Shawkey, "**Analysis and Design of a Reconfigurable Wideband I/Q Modulator and Ultra-Wideband I/Q Demodulator for Multi-standard Applications**", Microelectronics, vol. 102, August 2020, pp. 104830. IF=1.564
- Marwa Mansour, Abdelhalim Zekry, Mohammed K. Ali, and Heba Shawkey, "**A Reconfigurable Class-AB/F Power Amplifier for 0.1-4.2GHz Multistandard Applications**", Circuits, Systems, and Signal Processing, on line 24 august 2020. IF=1.68
- Marwa Mansour, Abdelhalim Zekry, Mohammed K. Ali, and Heba Shawkey, "**Analysis and Design of a 5G Multi-Mode Power Amplifier using 130 nm CMOS technology**", 2021 22nd Int'l Symposium on Quality Electronic Design(ISQED).
- Marwa Mansour, Abdelhalim Zekry, Mohammed K. Ali, and Heba Shawkey, "**Integrated multi-band RF transceiver design for multi-standard applications using 130 nm CMOS technology**", Microelectronics Journal, vol. 110 – no. 11, pp. 105006, April 2021. IF=1.564

Outlines

- **Introduction**
- **RF transceiver**
  1. Specification
  2. Architecture
- **Proposed Multiband High Efficiency Power Amplifier**
  1. Class-AB/F Power Amplifier design
  2. Post –layout Simulation Results
  3. Comparison with the State-of-the-Art
- **Proposed Wideband I/Q De/Modulator**
  1. UWB I/Q demodulator design
  2. Wideband I/Q Modulator design
  3. Comparison with the state-of-the art
- **Proposed Quadrature Voltage Controlled Power Oscillator**
  1. Quadrature voltage controlled power oscillator design
  1. Post –layout Simulation Results
  2. Comparison with the state-of-the art
- **Conclusions and future work**

Research objective

- Analysis and design high performance RF transceiver for LTE applications using 130 nm CMOS technology.
- Analysis and design the main parts of the RF transceiver, which consist of :

1. RF power amplifier
2. IQ Modulator
3. IQ Demodulator
4. Quadrature Voltage Controlled Oscillator

Long-Term Evolution (LTE)

- Frequency range from 0.7 to 3.8 GHz

1. bands 1 to 25 FDD
2. bands 33 to 43 TDD

- Modulation Schemes : QPSK, 16QAM, 64QAM
- Peak data rate in LTE :

1. UL: 75Mbps(20MHz bandwidth),
2. DL: 150Mbps(UE Category 4, 2x2 MIMO, 20MHz bandwidth),
3. DL: 300Mbps(UE category 5, 4x4 MIMO, 20MHz bandwidth)

- MIMO (Multiple Input Multiple Output) :

1. UL 1x2 1x4
2. DL 2x2 4x4

- Channel bandwidths (MHz) : 1.4, 3, 5, 10, 15, 20

RF transceiver

- The LTE (FDD) transmitter and receiver characteristics are specified by the LTE standard

LTE (FDD) Transmitter Characteristics

Parameter	UE/ Mobile/Portable Station
Channel Bandwidth (MHz)	1.4, 3, 5, 10, 15 and 20 MHz
Output Power (EIRP) (dBm)	23 ± 2dB
ACLR_1 (First adjacent channel) (dBc)	-30 (LTE Channel BWs)
ACLR_2 (Second adjacent channel) (dBc)	-36 (LTE Channel BWs)

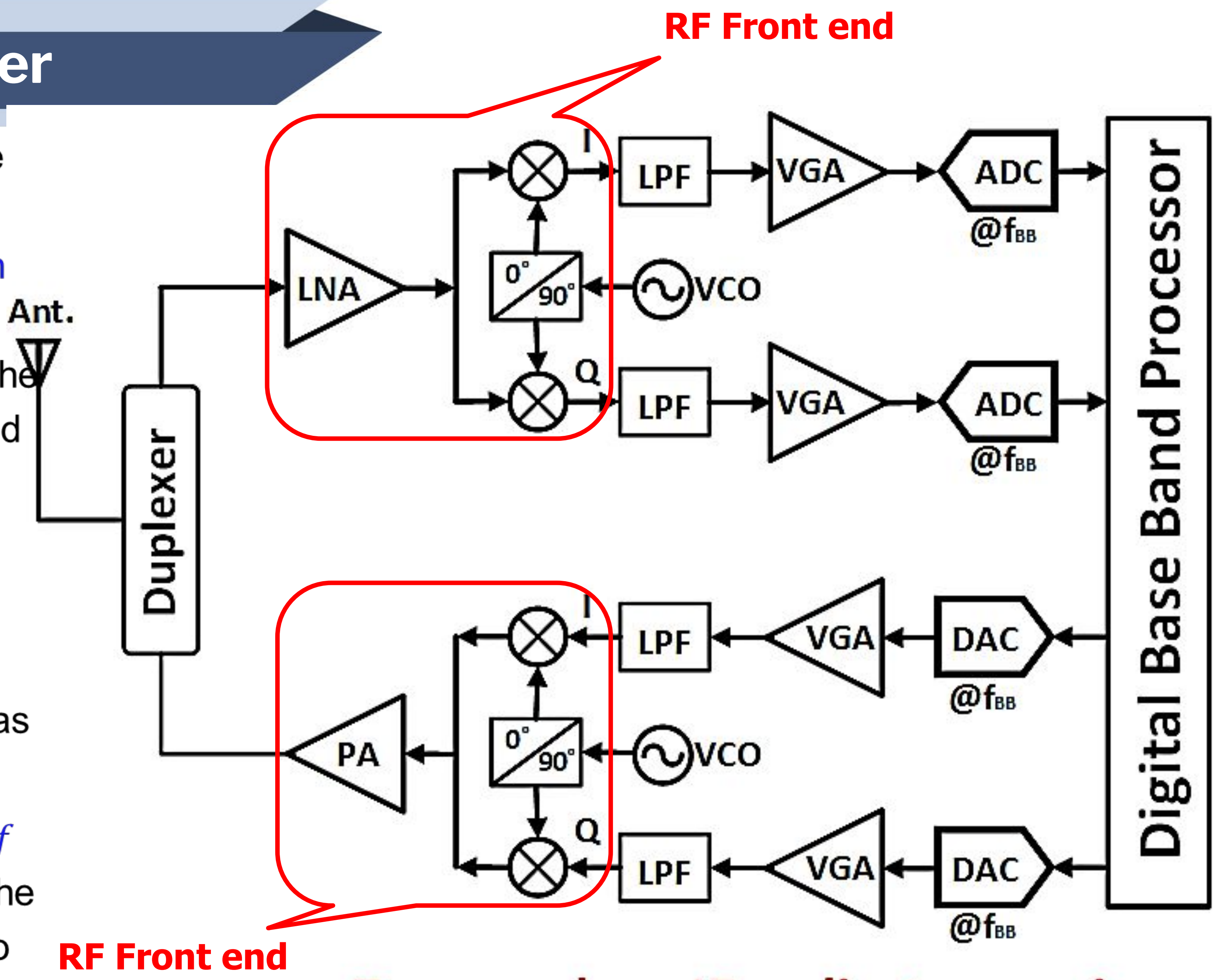
RF transceiver

LTE (FDD) Receiver Characteristics

Parameter	UE/ Mobile/Portable Station
Receiver Channel Bandwidth (MHz)	1.4, 3, 5, 10, 15 and 20
Receiver Temperature (kBT) (dBm)	-113.6, -109.7, -107.4, -104.4, -102.7, -101.4
Receiver noise Figure (dB)	12
Receiver Thermal Noise Level (dBm)	-101.6, -97.7, -95.4, -92.4, -90.7, -89.4
Reference Sensitivity (dBm) $P_{REFSENS}$ for Wide Area BS	-101.7, -98.7, -97, -94, -92.2, -91

Low-IF transceiver architecture

- The target of low-IF trx architecture is to combine the advantages of heterodyne and zero-IF trx i.e. high performances and high degree of integration at the same time, also the number of elements is reduced, and the cost is decrease.
- The IF frequency in low-IF trx architecture is usually selected as twice the Ch. BW.
- The RF part of low- IF trx is same as in zero-IF trx.
- The dc-offset, LO-leakage, and $1/f$ noise problem are relaxed due to the non-zero IF frequency compared to zero-IF trx.



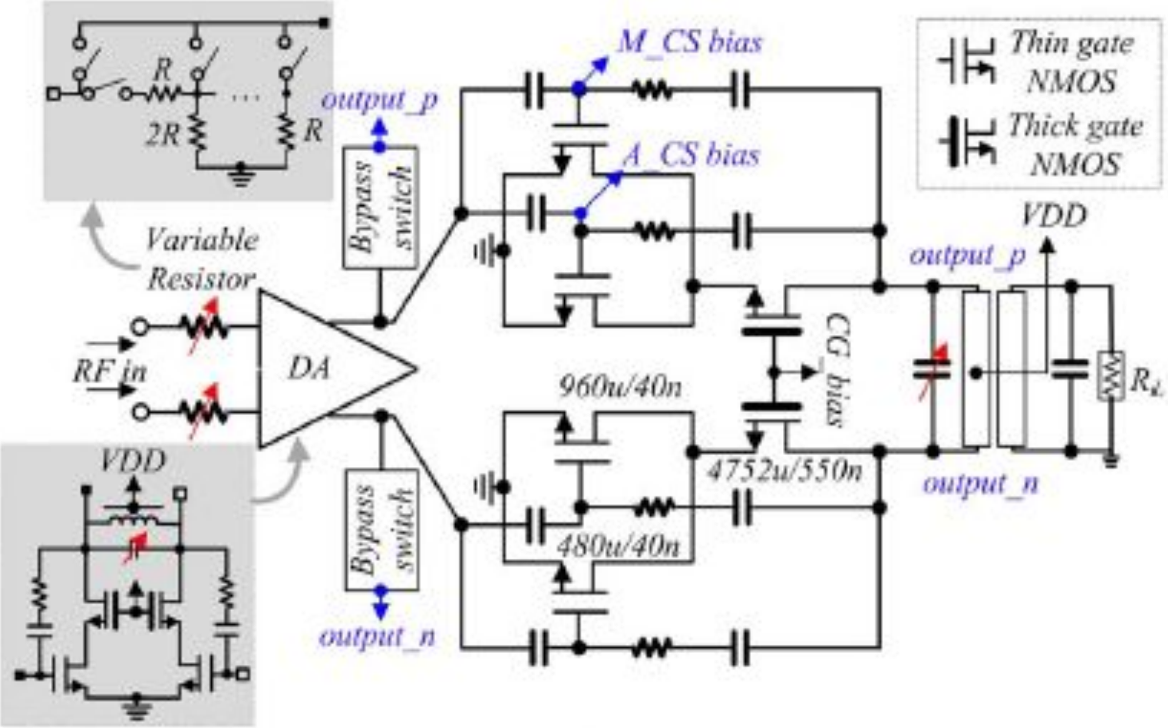
Zero- or low-IF radio transceiver

1

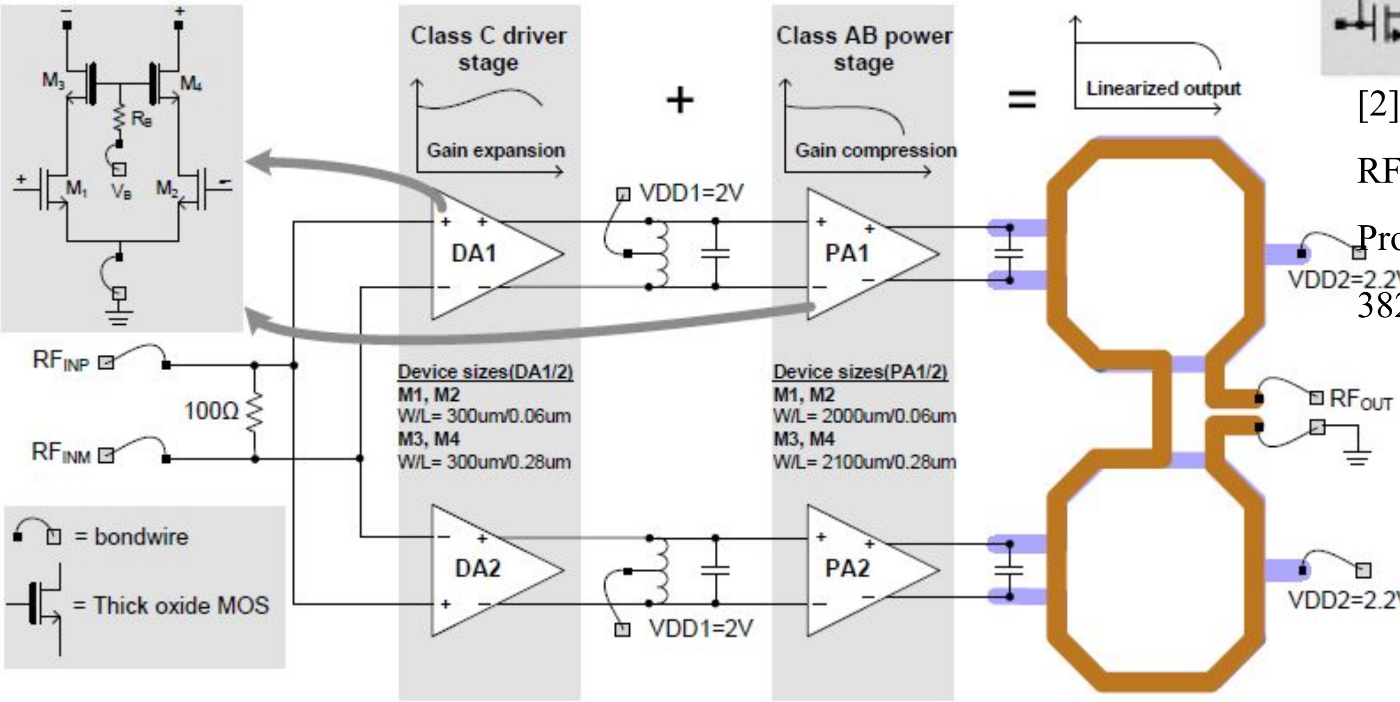
Proposed Multiband High Efficiency Power Amplifier

Previous work

- There are several design methods for wideband RF power amplifier which provides wideband matching,
- example for wide input matching, [1]-[2] used fixed and variable resistances that caused losses and consequently reduced the RF output power.



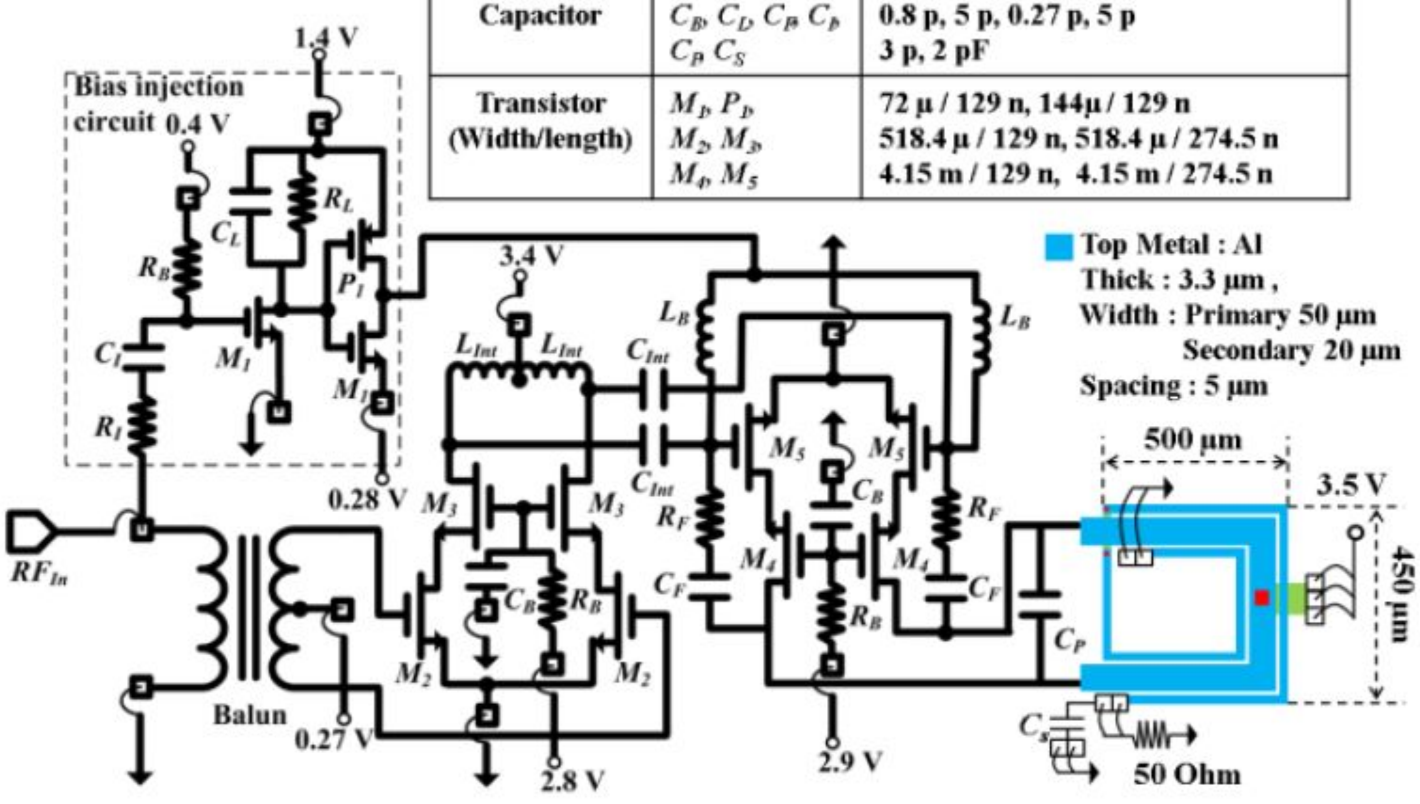
[2] N. Ryu, B. Park and Y. Jeong, "A Fully Integrated High Efficiency RF Power Amplifier for WLAN Application in 40 nm Standard CMOS Process," IEEE Microw.Wireless Compon. Lett., vol. 25, no. 6, pp. 382-384, June 2015.



[1] W. Ahmad, L. Xu, M. Törmänen and H. Sjöland, "A fully integrated 26 dBm linearized RF power amplifier in 65nm CMOS technology, "2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015, pp. 1306-1309.

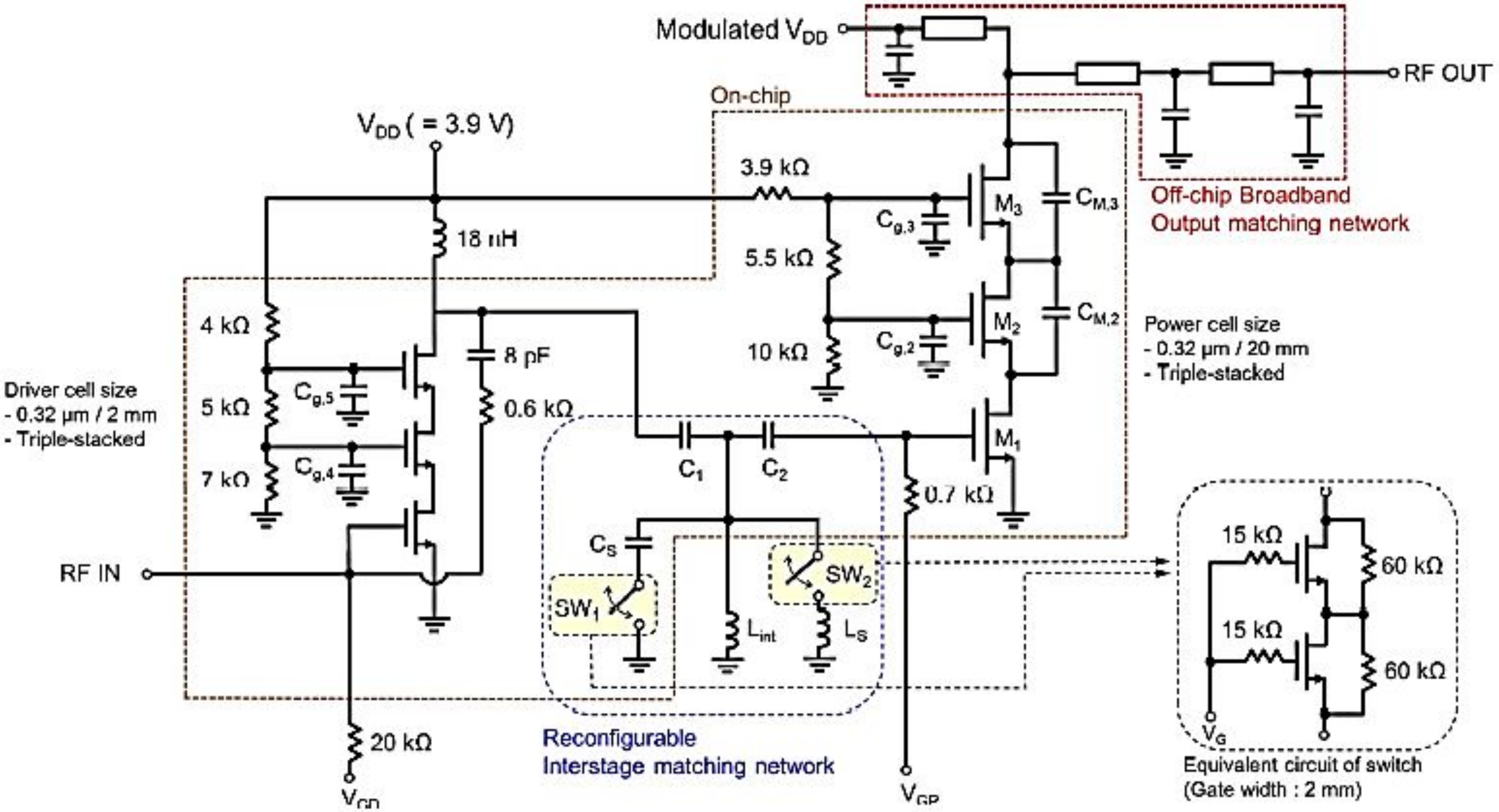
Previous work cont.

- For a wide inter-stage matching, on-chip inductor with poor quality factor and large area was used in [3]-[4], it achieved only narrow bandwidth less than 0.5 GHz.



[3] K. Kim, J. Ko, S. Lee and S. Nam, "A Two-Stage Broadband Fully Integrated CMOS Linear Power Amplifier for LTE Applications," **IEEE Trans. Circuits Syst II**, Exp. Briefs, vol. 63, no. 6, pp. 533-537, **June 2016**.

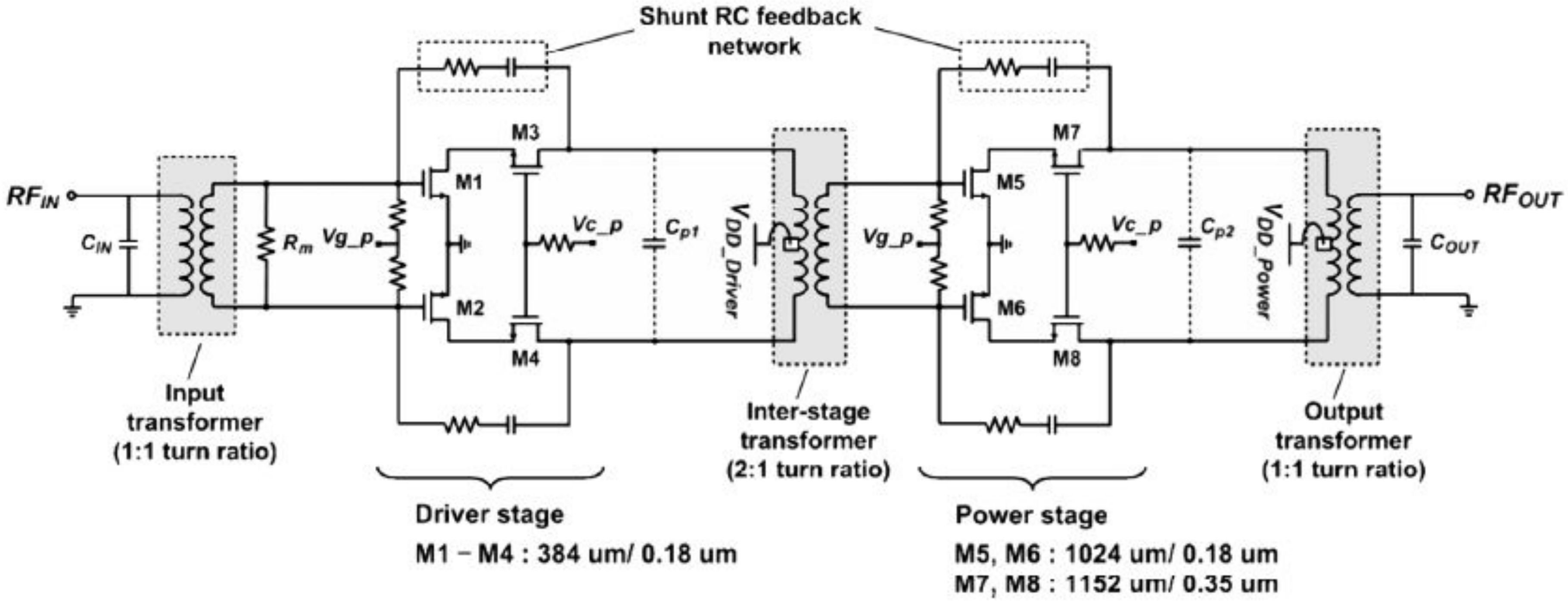
Previous work cont.



[4] S. Park, J. Woo, U. Kim and Y. Kwon, "Broadband CMOS Stacked RF Power Amplifier Using Reconfigurable Interstage Network for Wideband Envelope Tracking," **IEEE Trans. Microw. Theory Tech.,** vol. 63, no. 4, pp. 1174-1185, **April 2015**.

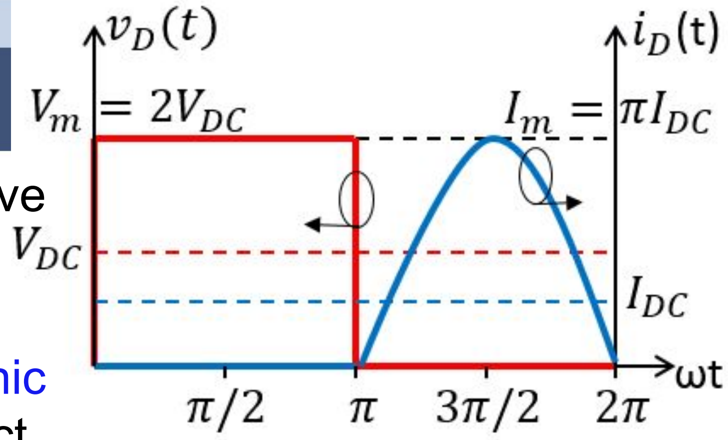
Previous work cont.

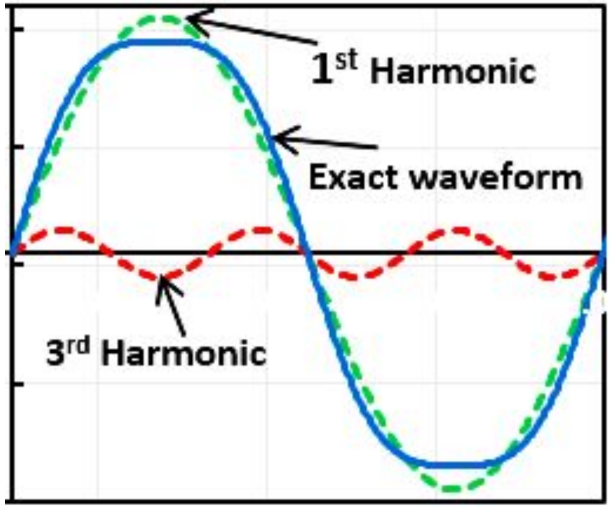
- In [5], on-chip transformer was used for wide input and inter-stage matching in the X-band and this method is not recommended at low frequency. bandwidth is 6.5 GHz (6.5–13 GHz).



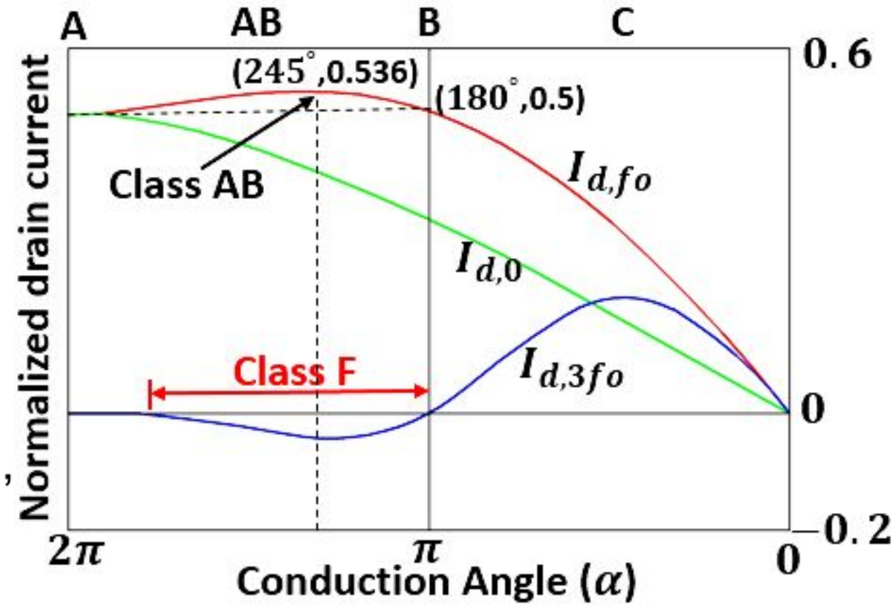
[5] B. Ku, S. Baek and S. Hong, "A Wideband Transformer-Coupled CMOS Power Amplifier for X-Band Multifunction Chips," **IEEE Trans. Microw. Theory Tech**., vol. 59, no. 6, pp. 1599-1609, **June 2011**.

Class-AB/F Concept





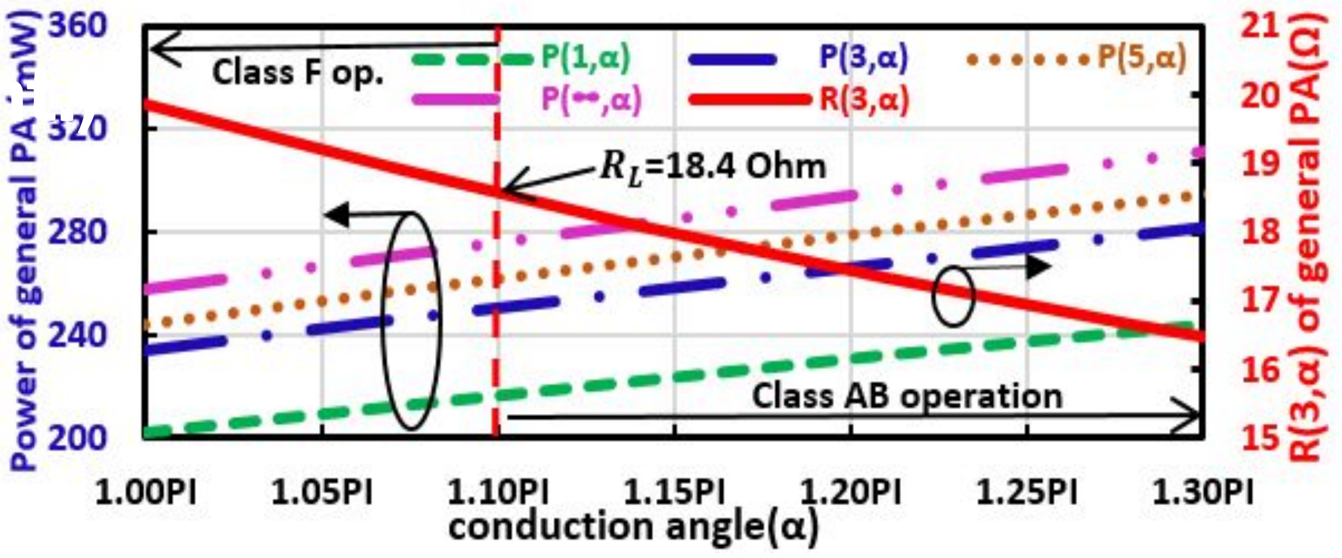
- The class-F is defined when half-rectified sine wave current and square wave voltage at the active device output.
- For flatten the voltage waveform, the third-harmonic component must have opposite phase with respect to the fundamental component.
- In class-AB, the current and voltage across output device have sinusoidal or partially sinusoidal waveforms
- The normalized amplitudes of I_d harmonic components at DC, f_o, and $3f_o$ as a function of α.
- Class-F operation if the bias point is selected in the range from device threshold to class-A
- Biasing the device below V_{th} (class-C) cannot lead to class-F operation, because in phase voltage harmonic components.
- Class-B bias point cannot be selected for a class-F due to the current waveform does not contain any odd harmonic components.
- For class-F operation α must be little above π and the device is biased just above V_{th}. For class-AB operation α must be between π and 2π, and the device is biased as well above V_{th}.

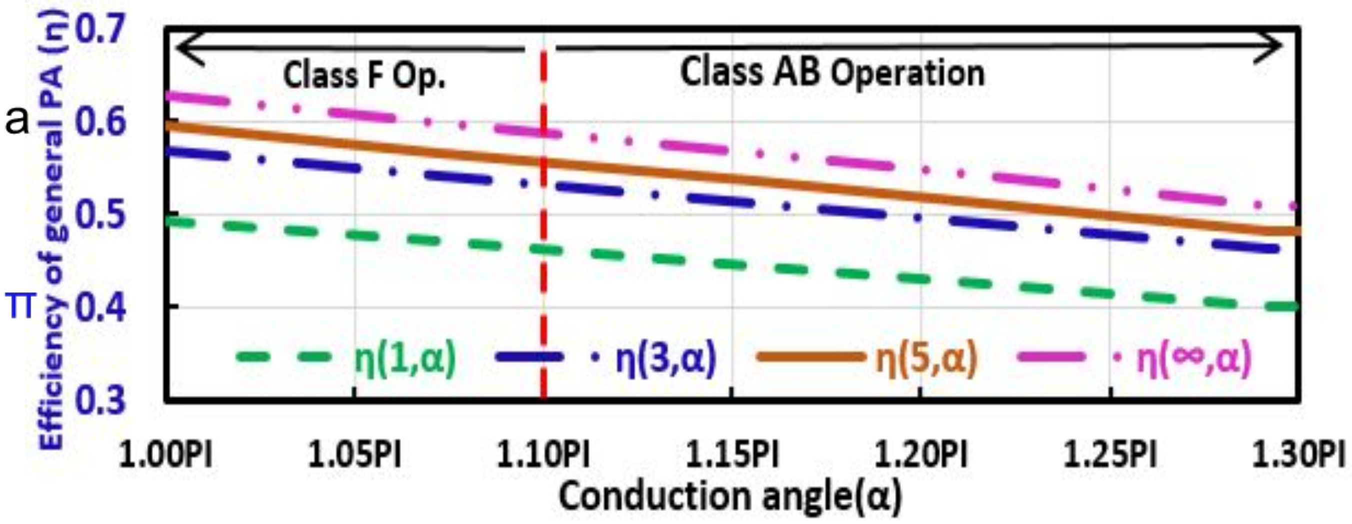


Class-AB/F Concept (co

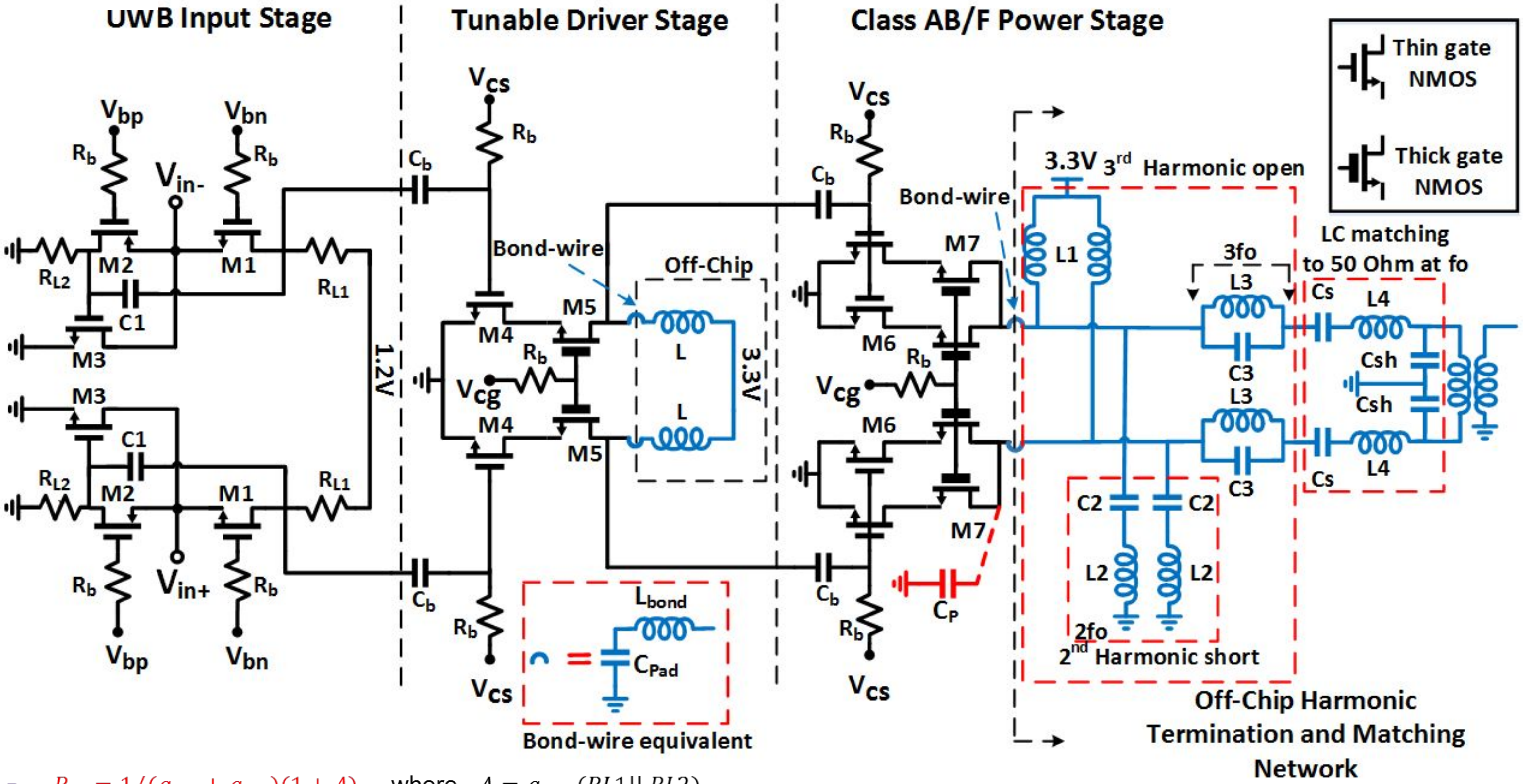
- $R_L = {V_1}^2/2P_{out} = (\delta_v(n)\ (V_{DC} - V_k))^2/2P_{out}$
- $R_L(n,\alpha) = \frac{\delta_v(n)\cdot V_{1\_max}}{I_{max}} \cdot \frac{2\pi(1-\cos(\frac{\alpha}{2}))}{(\alpha - sin\alpha)}$
- $P(n,\alpha) = \frac{I_{max}}{4\pi} \cdot \delta_v(n)(V_{DC} - V_k) \cdot \frac{(\alpha - sin\alpha)}{1-cos(\frac{\alpha}{2})}$
- $\eta(n,\alpha) = \frac{P(n,\alpha)}{P_{DC}(\alpha)} = \frac{\delta_v(n)\cdot(V_{DC}-V_k)}{V_{DC}} \cdot \frac{\alpha - sin\alpha}{4(sin\frac{\alpha}{2} - \frac{\alpha}{2}cos\frac{\alpha}{2})}$

- The output power and fundamental load of PA as a function of α and n at I_{max} = 330 mA, V_{DC} = 3.3 V, and V_k = 0.66 V.
- The efficiency of the PA over conduction angle of π to 1.3π.
- The Class-F amplifier has higher efficiency and less output power than the Class-AB amplifier as shown in Figures.





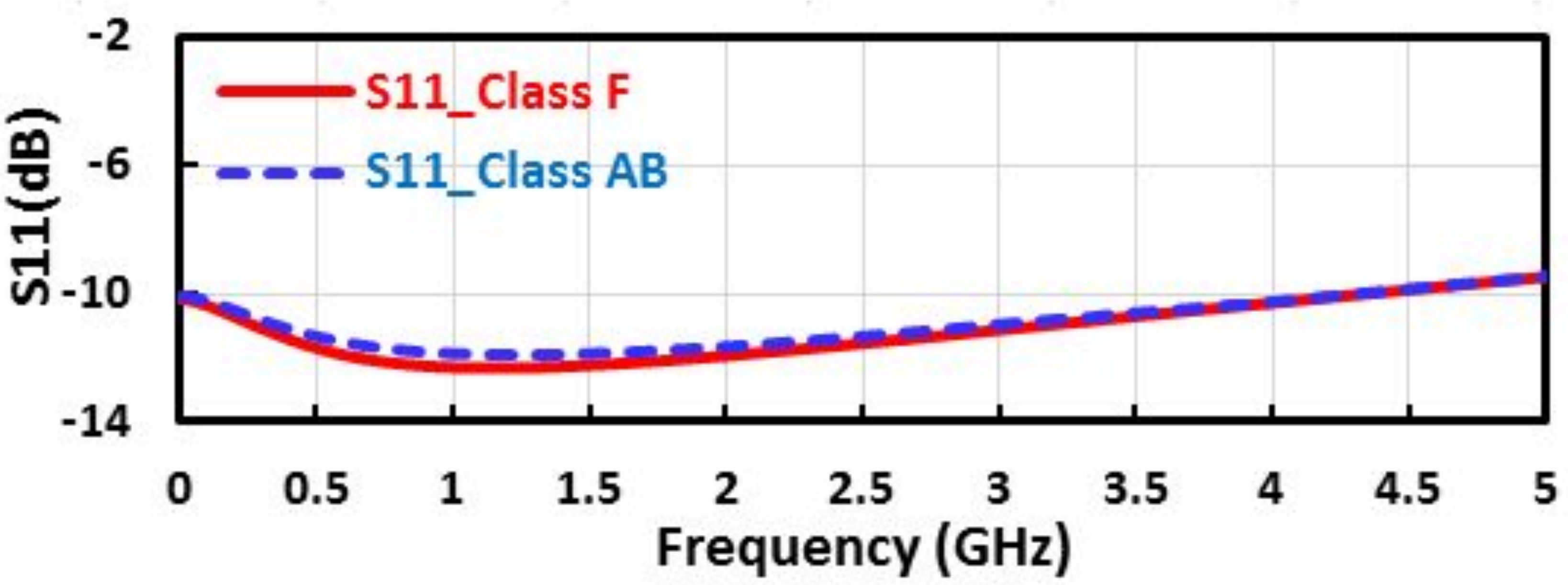
Proposed Power Amplifier Schematic



- $R_{in} = 1/(g_{m1} + g_{m2})(1 + A)$ where $A = g_{m3}\ (RL1 || RL2)$

Input return loss of the proposed PA

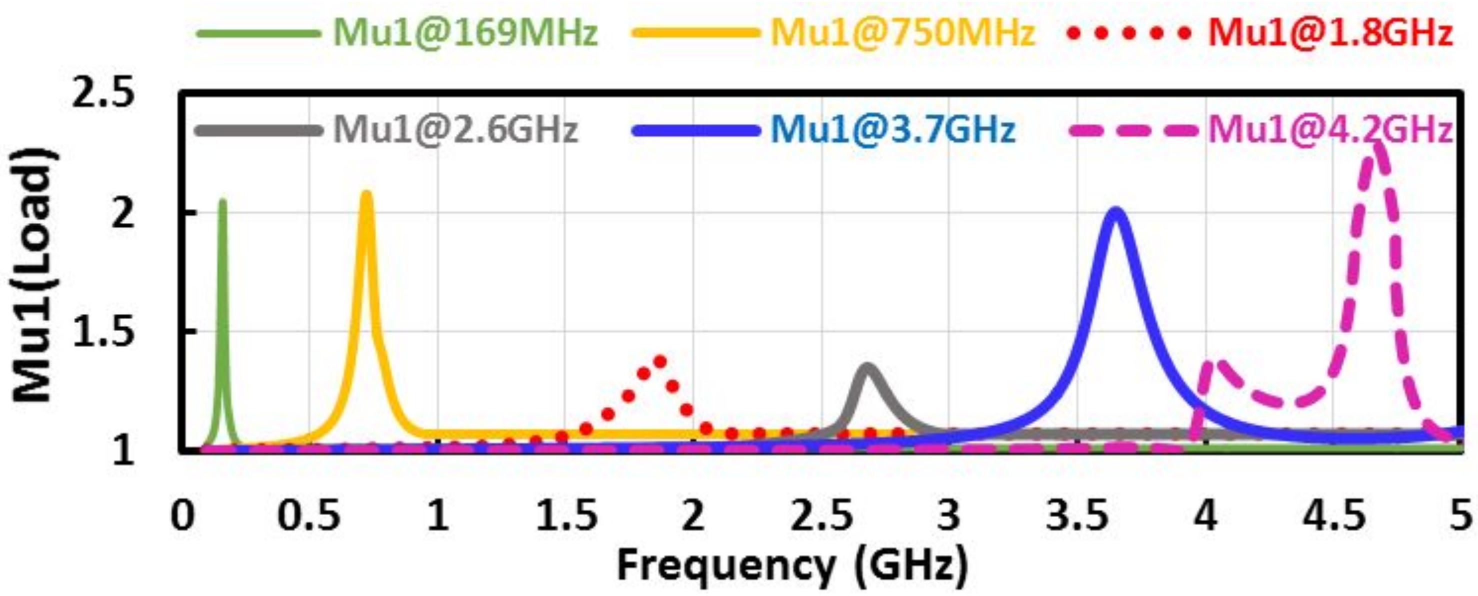
- Low voltage devices are used in the input stage to reduce the overall DC power consumption. The input stage provides constant gain over the frequency band and consumes a DC power of 3 mW.
- The inputs of both operation modes are matched to 50 Ohm over frequency from 0.1-5 GHz.



The stability of the proposed PA

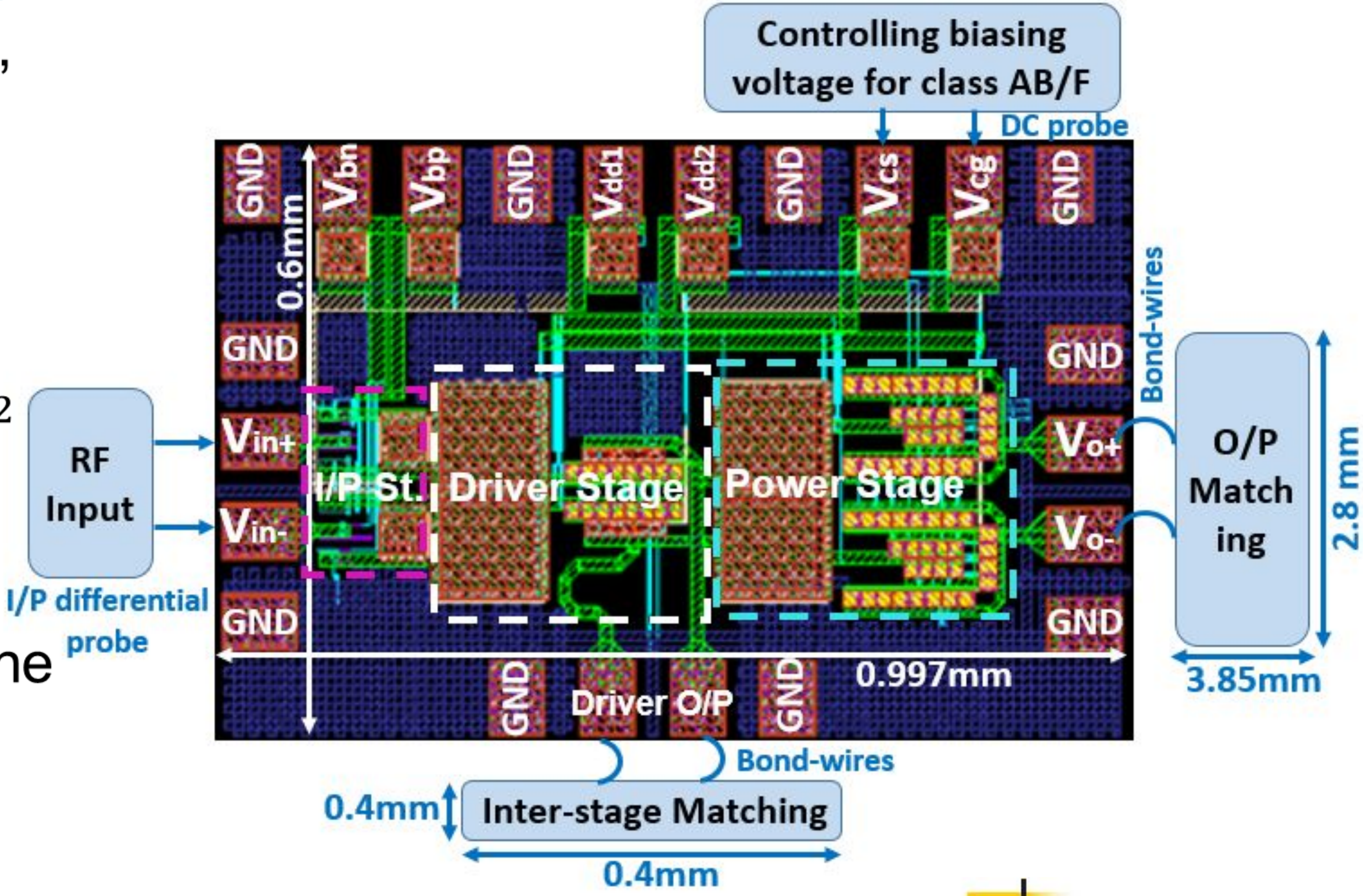
- The stability of the proposed PA is tested using Mu1 (Load) Stability factor test .
- $Mu1(Load) = \frac{1-|S_{11}|^2}{\ldots} > 1$

The proposed PA stability at each frequency band



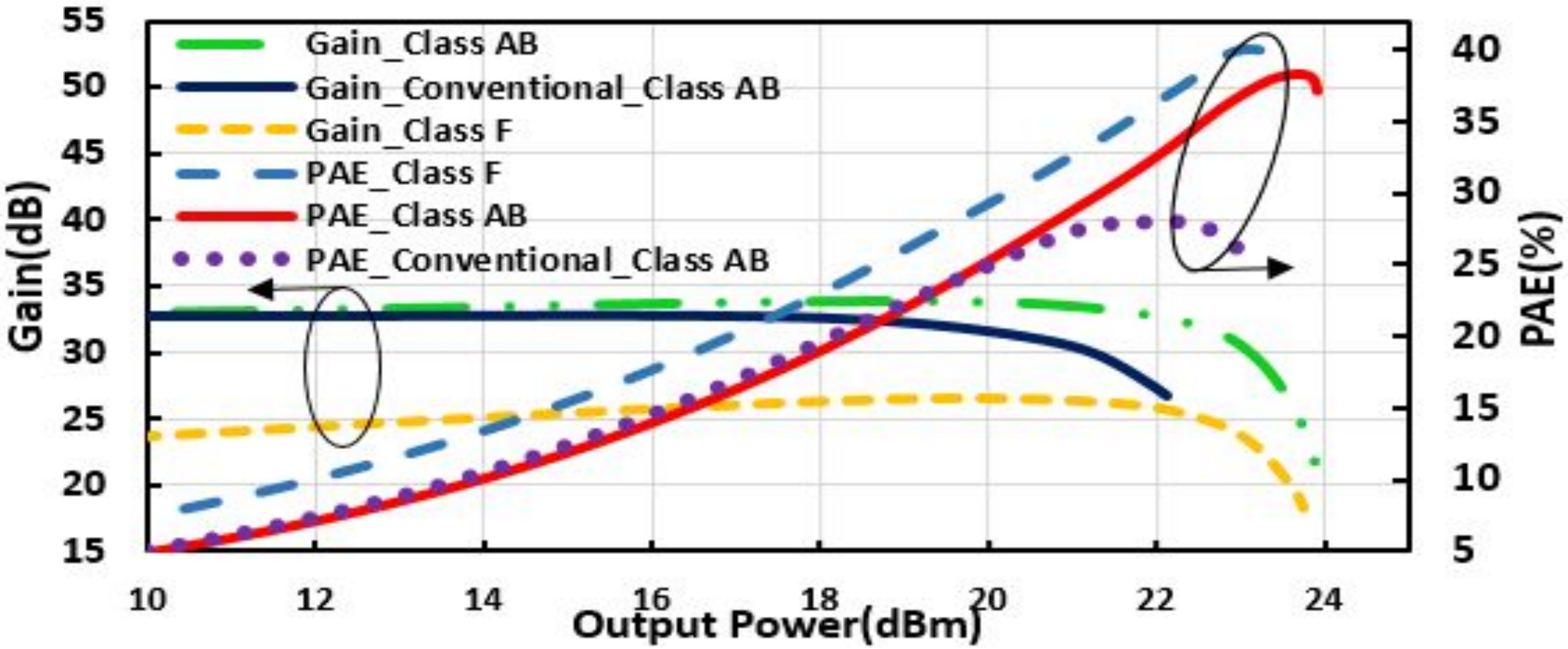
Post –layout Simulation Results

- The area of input, driver, and power stages are 0.03, 0.08, and 0.096 mm^2, respectively.
- The proposed PA has
  1. A chip area of 0.64 mm^2 including probing pads,
  2. Cell area 0.218 mm^2.
  3. The estimated area of the off-chip components equals 13.3 mm^2.



Post –layout Simulation Results (cont.)

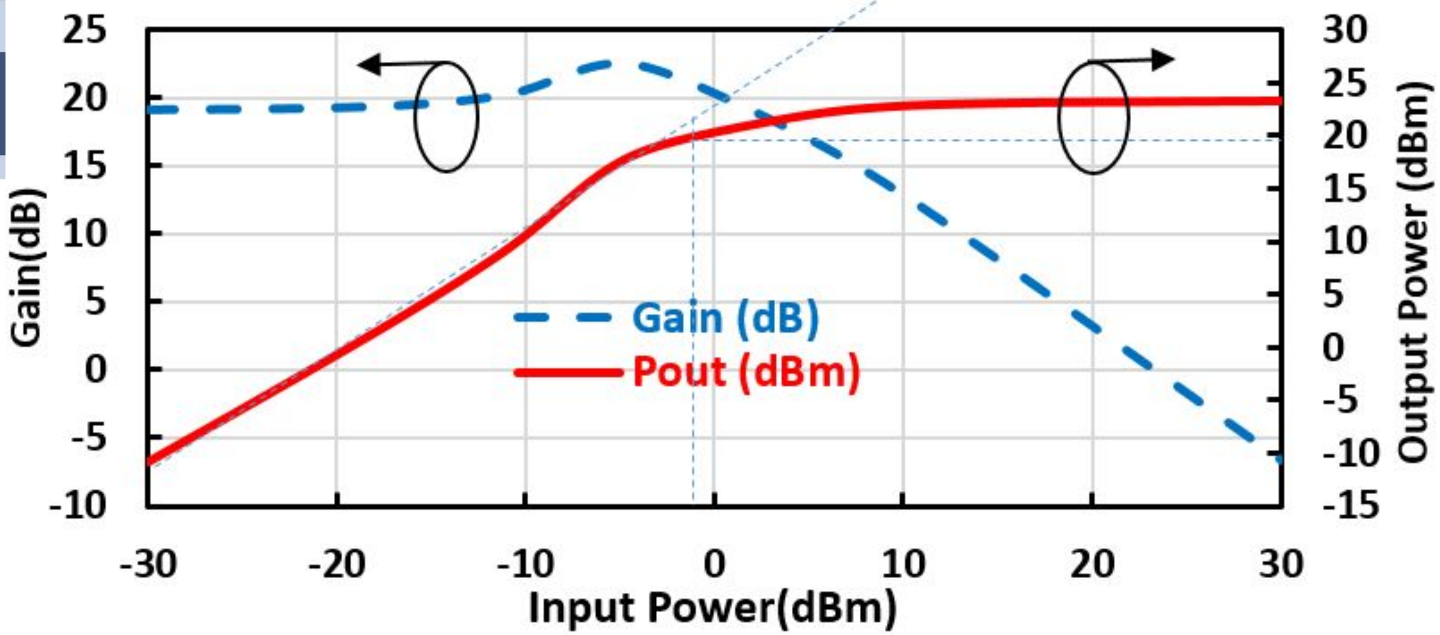
- A comparison between the proposed PA, and conventional class-AB PA.
- The conventional Class-AB PA has the second harmonic short circuit, and LC matching to 50 Ohm but does not have the third harmonic open circuit.

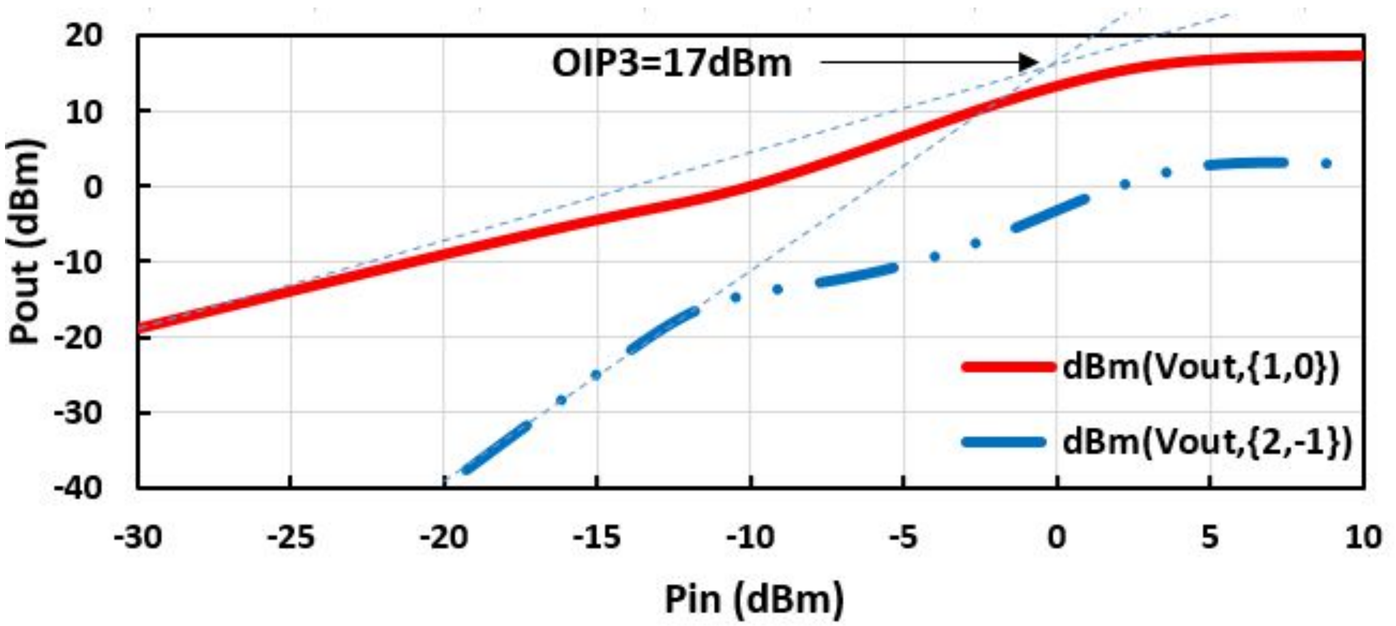


- Using the third harmonic open circuit in the proposed PA improves the PAE of the proposed class-AB PA by 10% over the conventional Class-AB PA, and this leads to the difference between PAE of the proposed PA class-AB and class-F is about 2% only.
- The output power of the proposed PA class-AB is improved by 1.5 dBm over the conventional Class-AB PA, and more linear.
- The gain of the proposed class-F PA is lower than that of the proposed class-AB PA because of the lower bias.

Post –layout Simulation Results

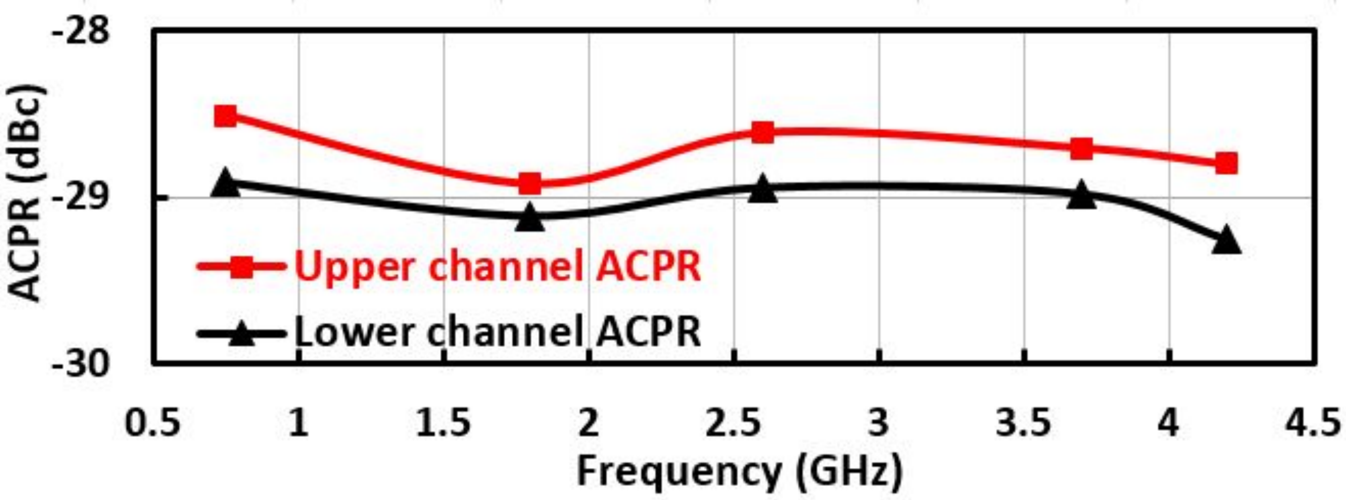
- The gain and output power versus input power of class-AB PA.
- OP_1dB=19.6dBm
- The OIP3 is modeled using two tone test, the fundamental and the third harmonic with swept input tones power.
- The OIP3 of the class AB equals 17 dBm at 1.8 GHz frequency band.

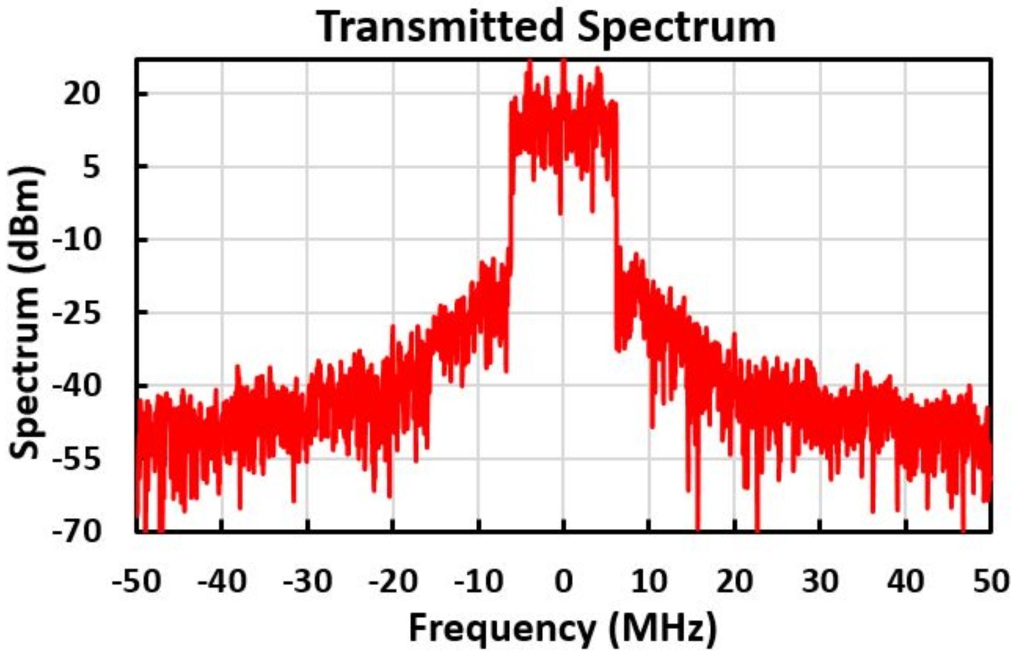




Post –layout Simulation Results (cont.)

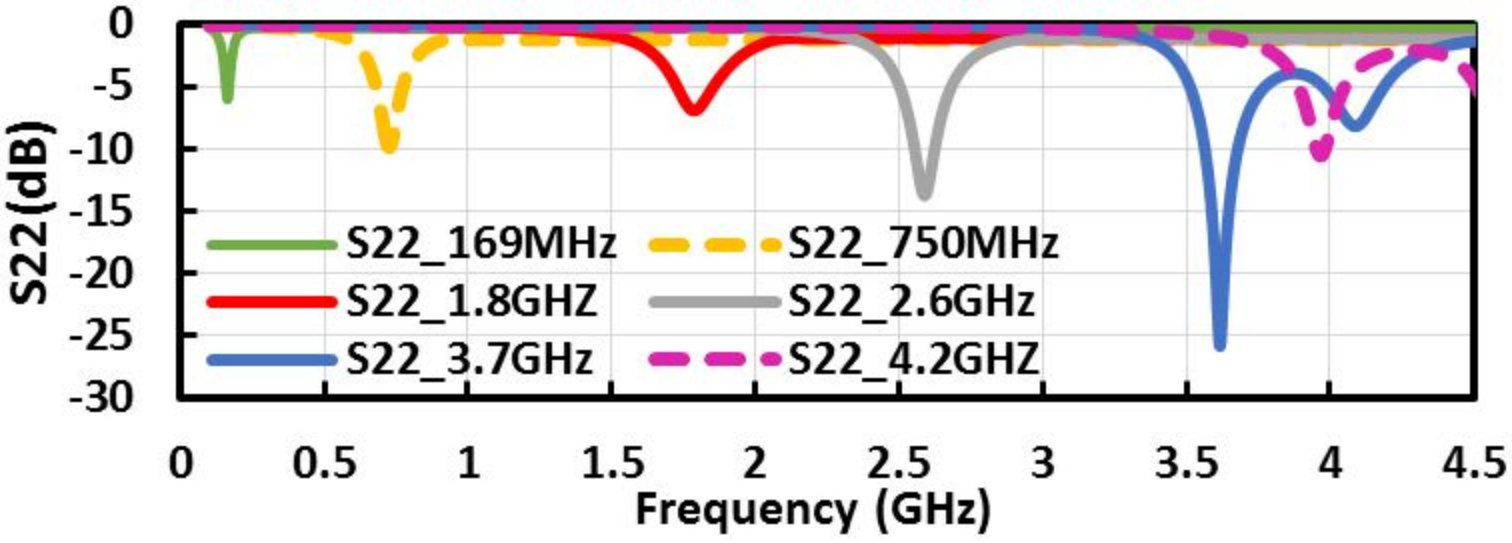
- The adjacent channel power ratio (ACPR) of the proposed class-AB PA, for LTE 15MHz Ch. BW over L frequency range from 0.7 to 4.2 GHz.
- The transmitted spectrum of the proposed class-AB PA with 1.8GHz centre frequency, and Ch. BW of 15MHz.



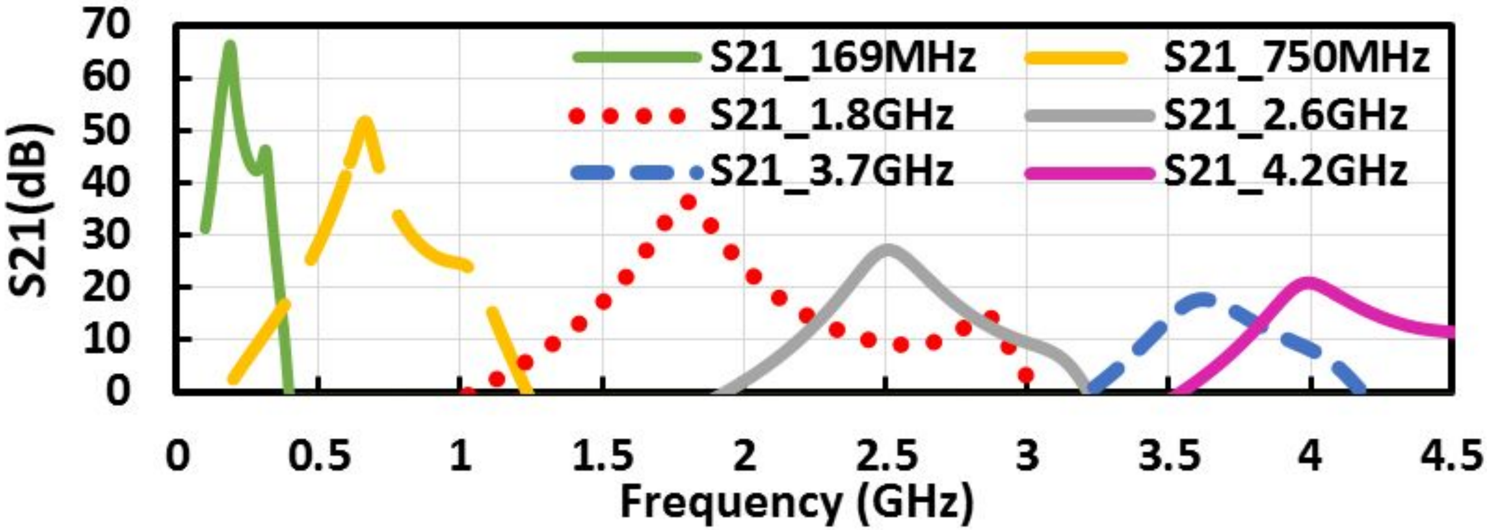


Post –layout Simulation Results (cont.)

- The output return loss (S22) a[…] each frequency band.

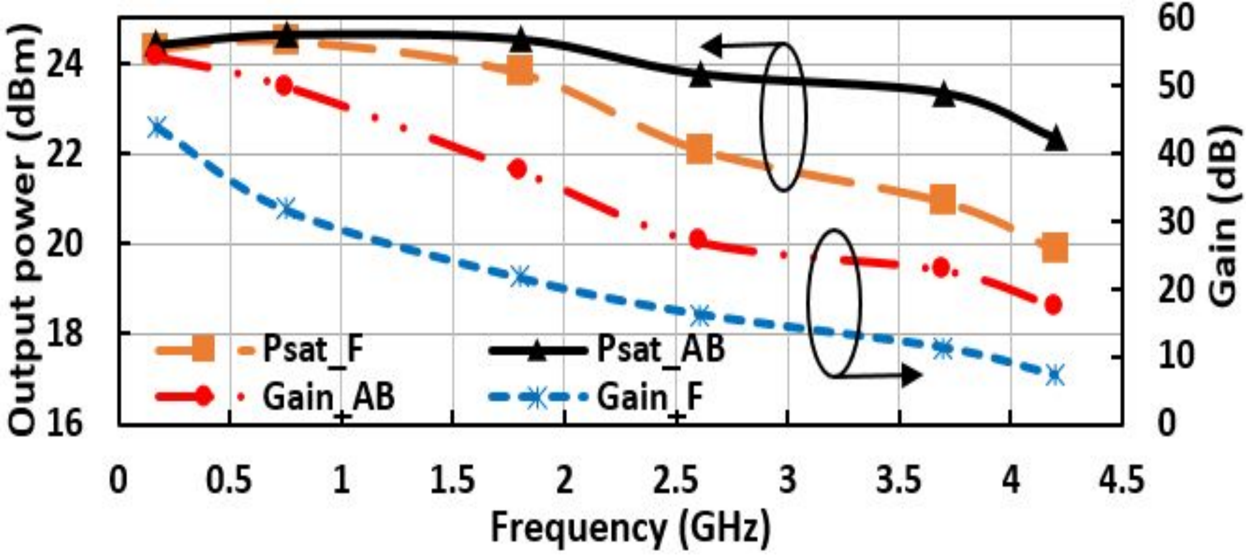


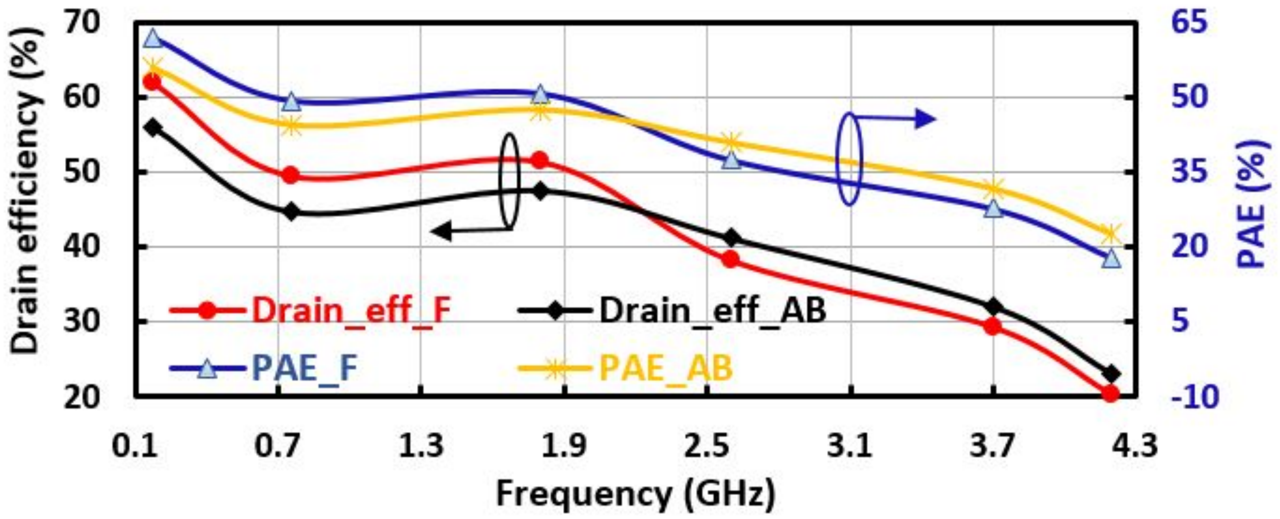
- the small signal gain (S21) at each frequency band of the proposed PA.



Post –layout Simulation Results (cont.)

- The saturated output power and the gain over frequency for the proposed PA .
- The PAE, and the drain efficiency are decreased with frequency.
- According to following equation drain efficiency is inversely proportional to frequency.
- $\eta_{drain} = P_{OUT}/P_{DC} = \pi/(4(1 + C_d R_L f_O))$





Comparison with the State-of-the-A

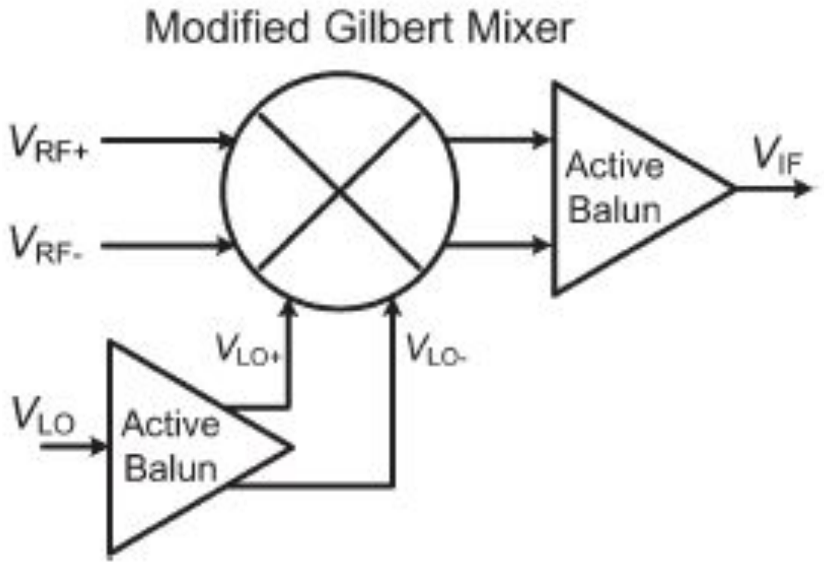
Index	This work		[6] IEEE Trans. Circuits Syst II (**2014**)		[7] IEEE Microw.Wireless Compon. Lett. (**2014**)	[8] IEEE Microw.Wireless Compon. Lett. (**2015**)	[9] IEEE Microw.Wireless Compon. Lett. (**2018**)	[10] IEEE Microw.Wireless Compon. Lett. (**2017**)
Freq.(GHz)	0.1-4.2		0.1-1.5		0.82-0.92	2.4	3/9	2
Mode	Linear	Switch	Linear	Switch	Switch	Linear	Linear	Linear
	24.6	24.5	20.5	23.2	26.7	24.6	24.8/21.5	24.5
	41	62.1	29	60	34.2	38 peak drain eff.	32.8/10.7	45.6
	164mW	16mW	391mW		NA	333.3mW	236/365mA 3.6V	NA
Technology	130 nm		65 nm		180 nm	40 nm	180 nm	180nm
Die area(mm^2)	0.218 PA core only		0.375 PA core only		1.41 all PA area	0.54	1.06/0.79 PA core only	0.94 PA core only
Fully integration	NO/with off-chip matching networks		NO/with off-chip matching networks		NO/with off-chip FB networks	YES	NO(series L-C W/bond wire)	NO/with off-chip components
ACPR(dBc)	-29.3/15MHz Ch. BW		NA		-30.3 /10MHz Ch. BW	NA	NA	-30/10MHz Ch. BW
Results	Post Layout Simulation		Measured		Measured	Measured	Measured	Measured

2

Proposed UWB I/Q Demodulator

Previous work

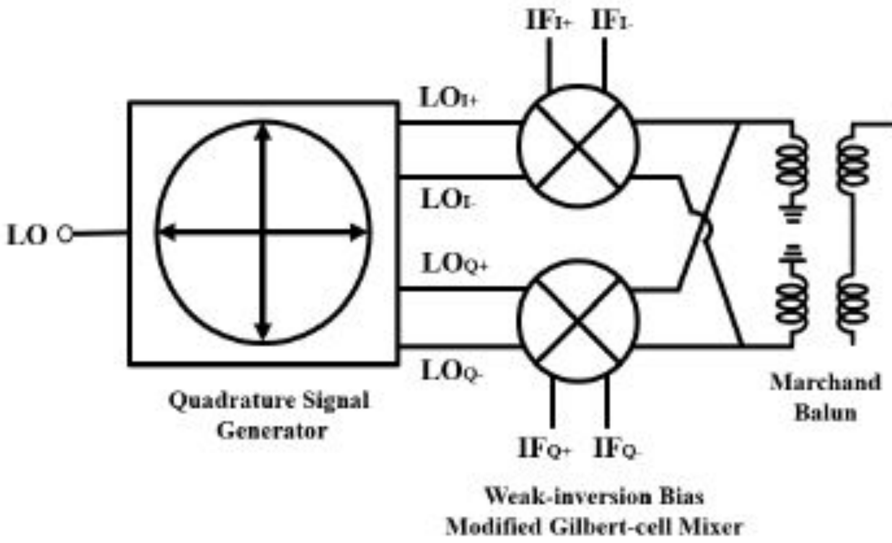
- There are many design techniques for wideband RF mixer which provide wideband characteristics.
- For example, wideband down-conversion mixer with active IF balun for matching is presented in [11], its conversion gain varies from 3 to 8 dB.



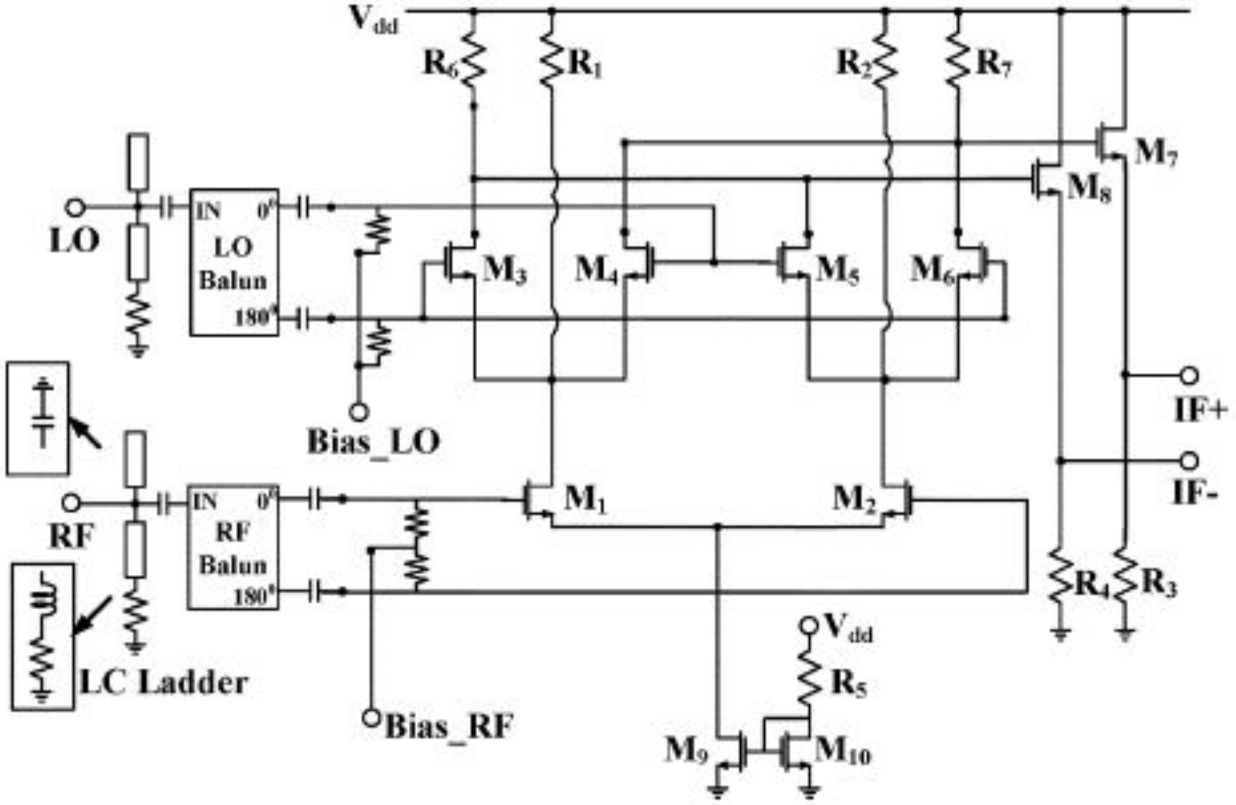
[11] H. Zijie and K. Mouthaan, "A 1- to 10-GHz RF and Wideband IF Cross-Coupled Gilbert Mixer in 0.13- um CMOS," in **IEEE Transactions on Circuits and Systems II**: Express Briefs, vol. 60, no. 11, pp. 726-730, **Nov. 2013**.

Previous work cont.

- In [12], down-conversion mixer with on-chip RF balun was used to achieve matching from 25 GHz to 75 GHz .
- In [13], an on-chip coupler and Marchand balun in the I/Q modulator are used covering a bandwidth of 34-39 GHz. The on-chip passive baluns and couplers are not recommended at low frequency as they have low quality factor and occupy large area.



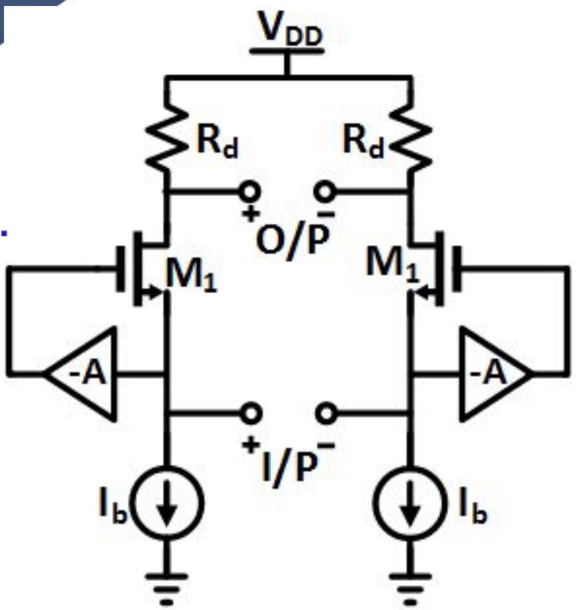
[13] C. Chen, J. Lin and H. Wang, “A 38-GHz High-Speed I/Q Modulator Using Weak-Inversion Biasing Modified Gilbert-Cell Mixer,” in **IEEE Microwave and Wireless Components Letters,** vol. 28, no. 9, pp. 822-824, Sept. 2018.



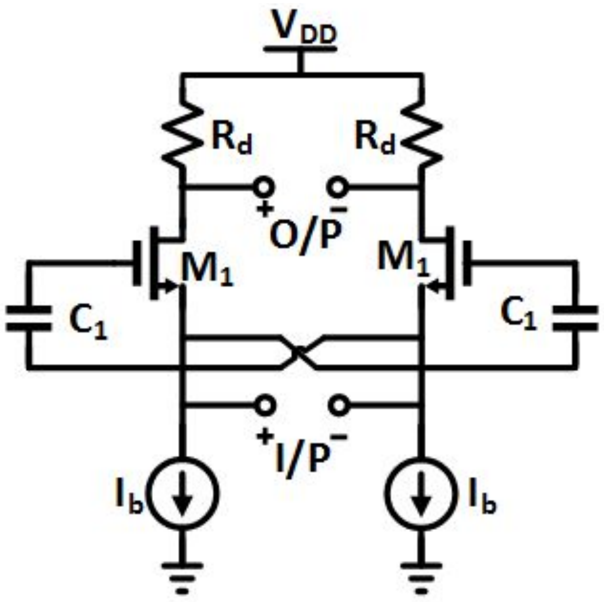
[12] J. Tsai, P. Wu, C. Lin, T. Huang, J. G. J. Chern and W. Huang, "A 25–75 GHz Broadband Gilbert-Cell Mixer Using 90-nm CMOS Technology,” in **IEEE Microwave and Wireless Components Letters**, vol. 17, no. 4, pp. 247-249, April **2007**.

Capacitive Cross Coupling (CCC) common gate configuration.

- G_m-boosting technique, a technique used to
1. enhance the transconductance by factor of (1+A).
2. reduces noise figure (NF)
3. decreases power consumption
- by the same factor compared to common gate configuration, where A is the boosting amplifier gain.
- The CCC common gate configuration is a specific case of G_m-boosting technique, where a passive unit gain is used as boosting amplification .
- where the negative amplification is specified by capacitor voltage divider as following;
- $A = \frac{C_1}{C_1 + C_{gs}} = \frac{1}{1 + \frac{C_{gs}}{C_1}}$ Thus if $C_1 \gg C_{gs}$ then $A \approx 1$ and
- $G_{m,eff,CCC} \approx 2 g_{mi}$



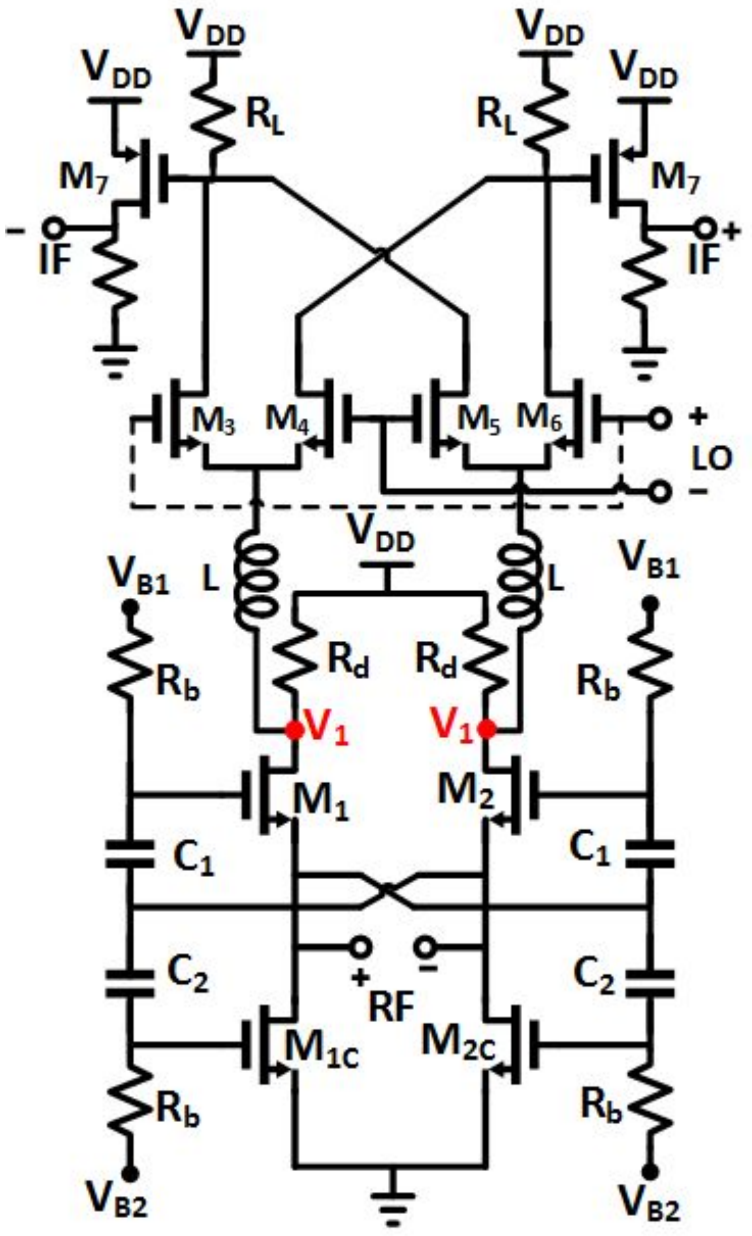
Gm-boosting configuration



Capacitive Cross Coupling (CCC) common gate configuration.

Proposed Down-Conversion Mixer

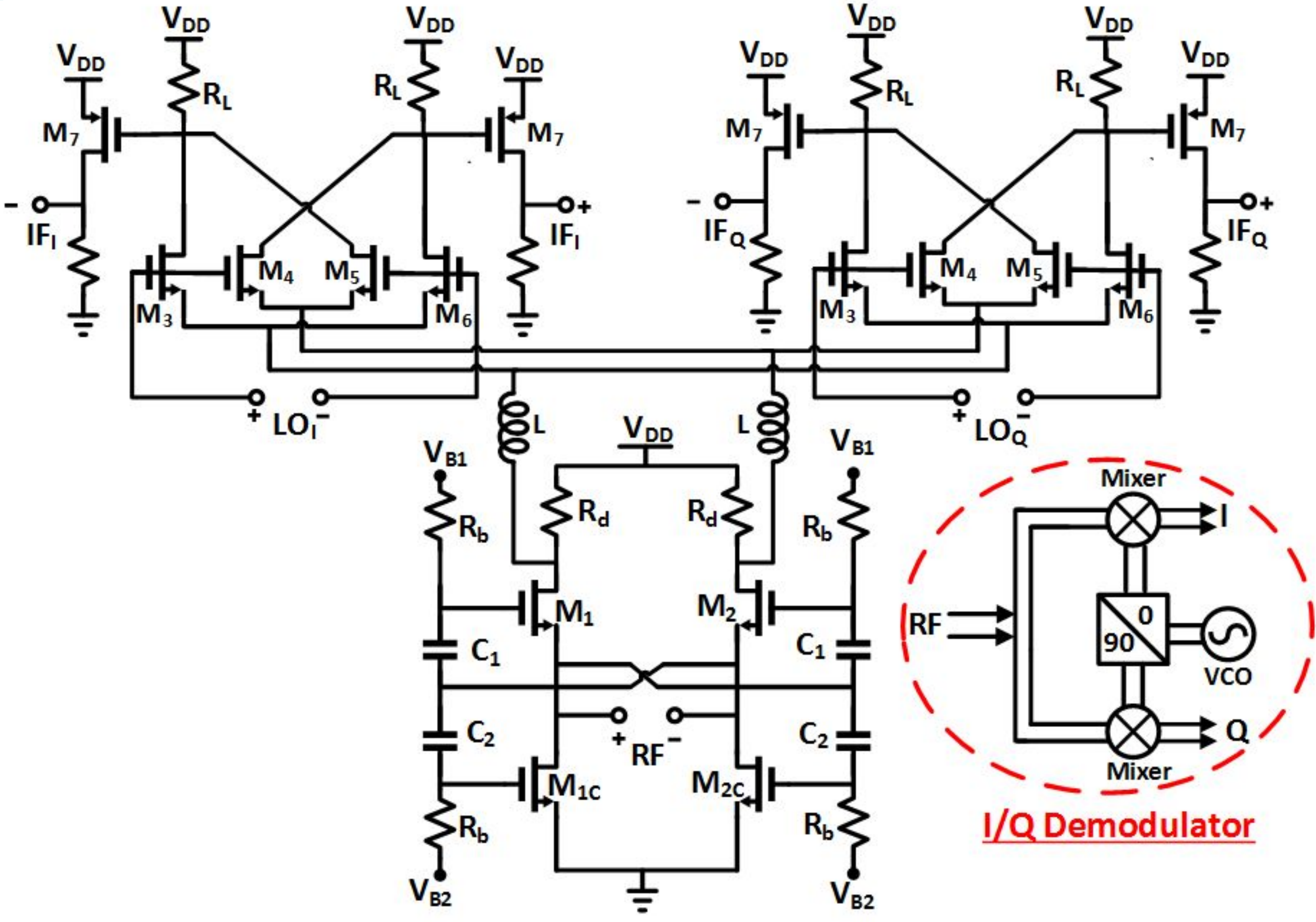
- The RF transconductance stage is a CCC common-gate configuration.
- The CCC common gate configuration has a transconductance equals to $2g_{m1,2}R_d$.
- The local oscillator (LO) switching transistors M_3–M_6, to perform frequency conversion.
- A PMOS common-source amplifier is used as a buffer.
- inductive peaking is used for bandwidth extension, a peaking inductor (L) is inserted between the RF stage and LO switching pairs (M_3–M_6).



Proposed CMOS I/Q Demodulator

- I/Q modulator consists of:

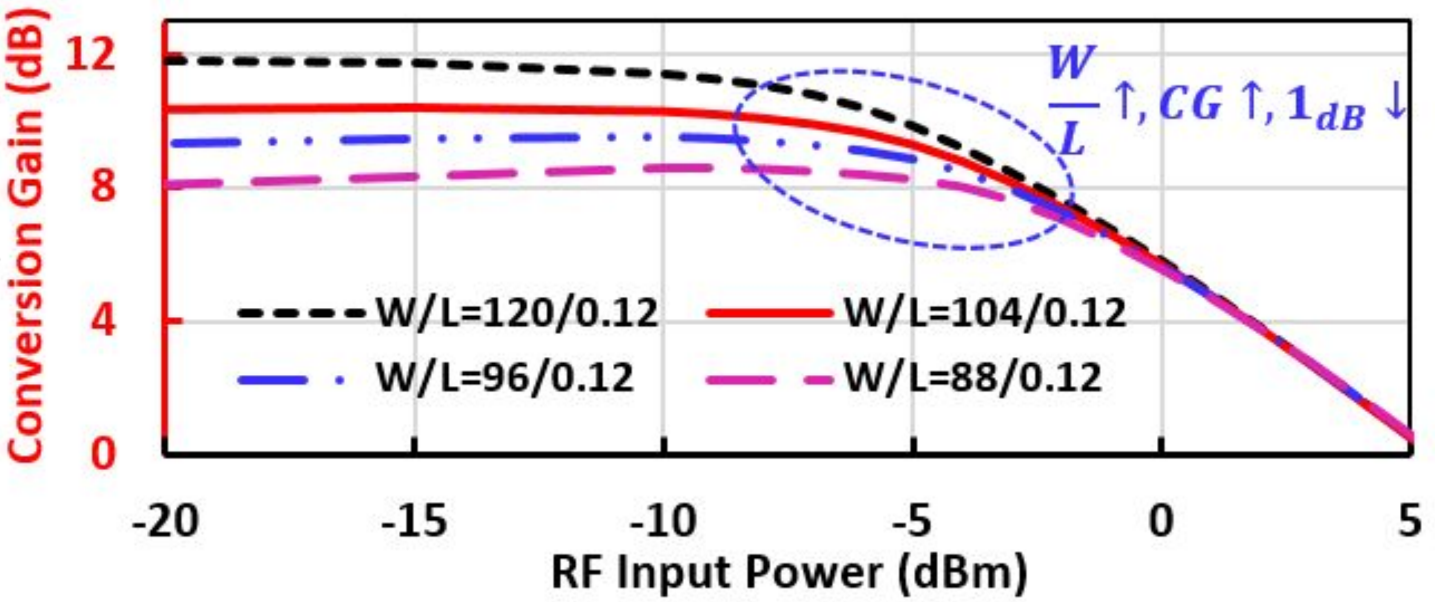
1. Low-noise transconductance stage (RF-stage)
2. Two down-conversion mixers for the I and Q channels.



CMOS I/Q Demodulator

Proposed CMOS I/Q Demodulator

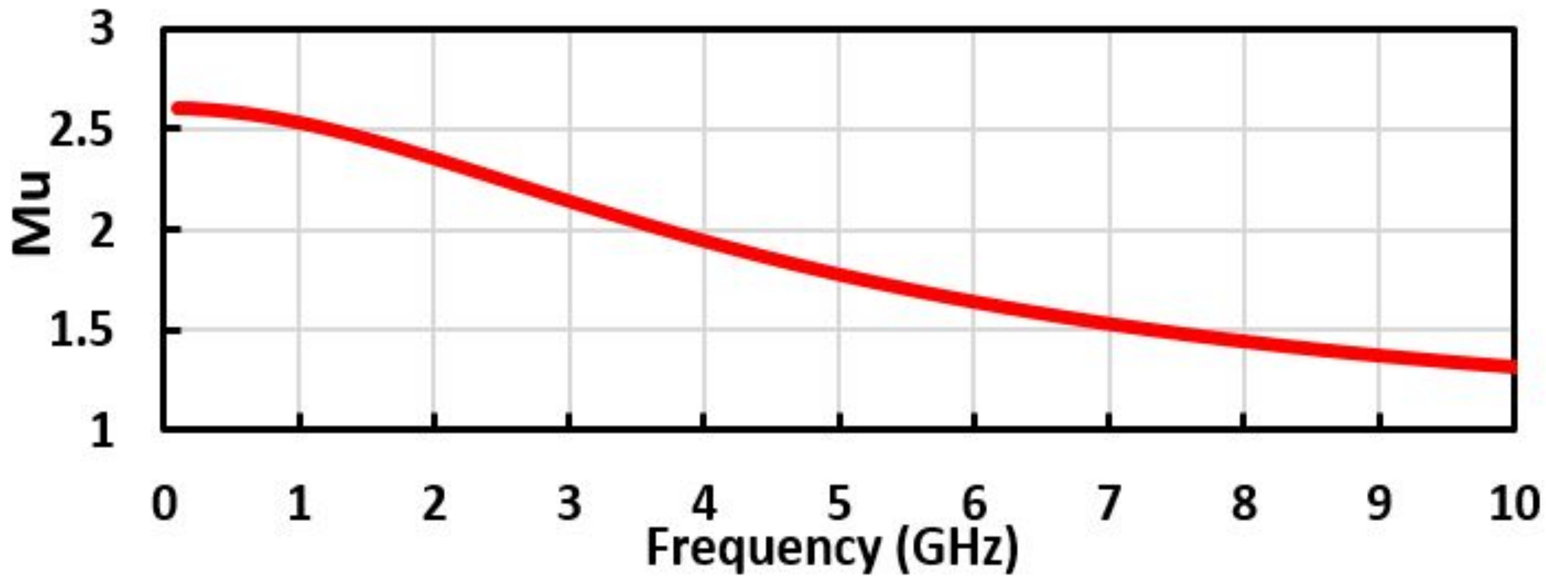
- The transistors size (W/L) was chosen to achieve maximum conversion gain (CG) with acceptable linearity. The CG and the linearity (IIP3) depend on transistors size as the following equations:



- $CG = \frac{2}{\pi} g_{m1,2} R_L \approx \frac{2}{\pi} R_L \sqrt{\mu_n C_{ox} \frac{W}{L} I_{Bias}}$
- $IIP3 \approx 4\sqrt{\frac{2}{3}\frac{I_{Bias}}{\mu_n C_{ox}\frac{W}{L}}}$

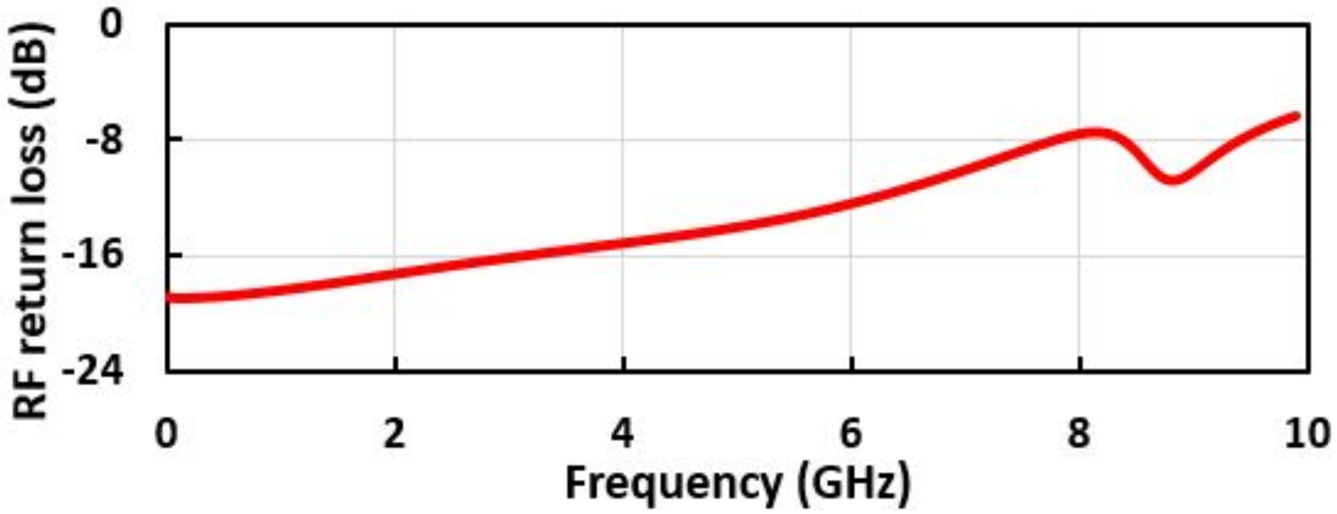
- The value of R_L was selected in a trade-off between the CG and the transistor headroom. The CG is increased with R_L, nevertheless, this increases the voltage drop across R_L leading to less headroom across the transistors M_{1-2} .

Stability of the CCC common gate



- The stability of the capacitor cross-coupling (CCC) common gate configuration stage is tested using Mu factor that is calculated using equation.
- $Mu = \frac{1-|S_{11}|^2}{|S_{22}-S^*{}_{11}\cdot\Delta|+|S_{12}\cdot S_{21}|} > 1$
- Where $\Delta = |S_{11}.S_{22} - S_{12}.S_{21}|$, S_{11} is input return loss, S_{22} is output return loss, S_{12} is reverse transmission, and S_{21} is forward transmission.

RF input return loss of the proposed I/Q Demodulator

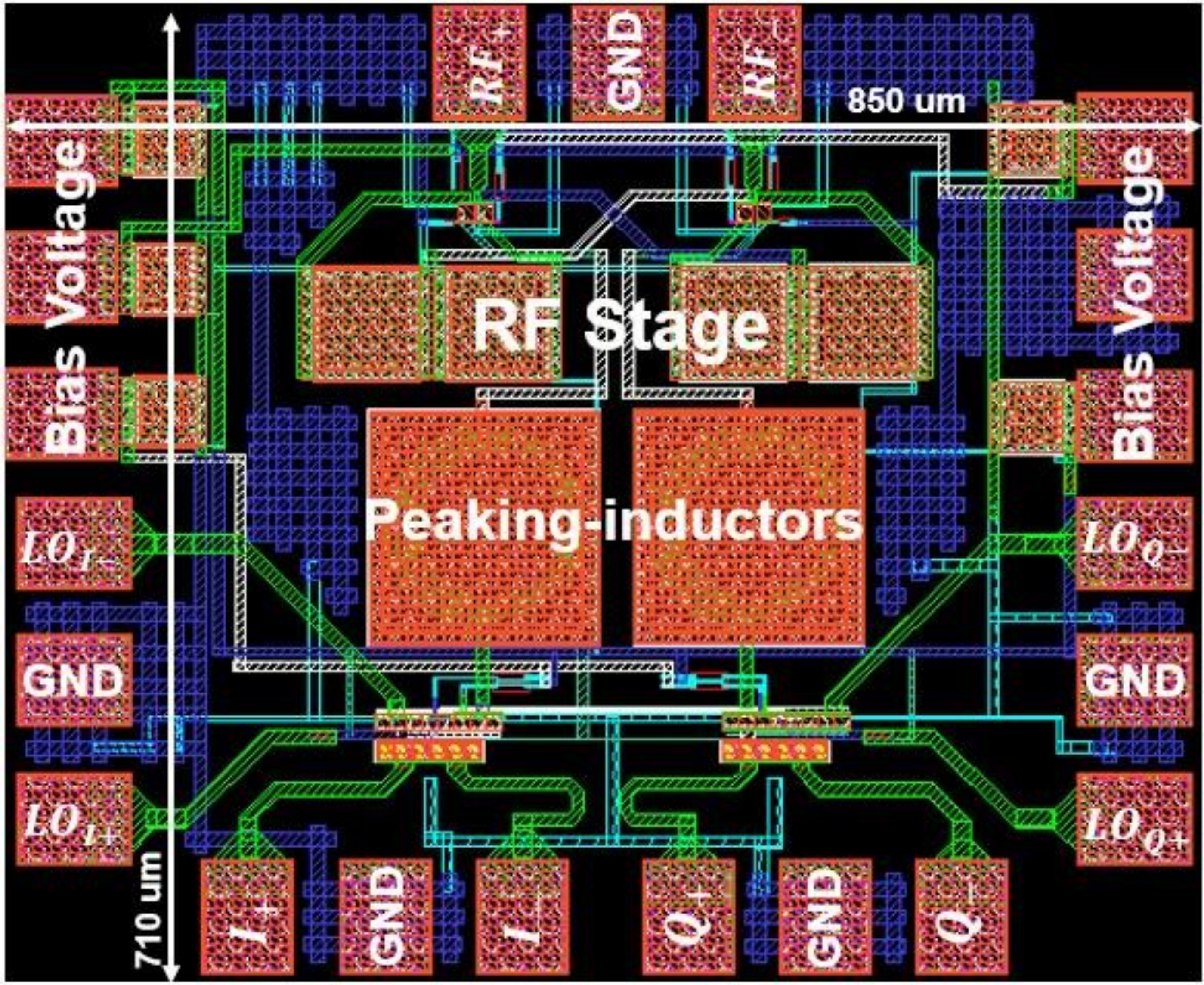


- The RF differential input resistance of the proposed I/Q demodulator are determined by $R_{in-diff} = 2/2g_{m1,2}$. The RF input return loss is less than -8 dB over wide frequency range from 0 to 10 GHz.

I/Q Demodulator Layout

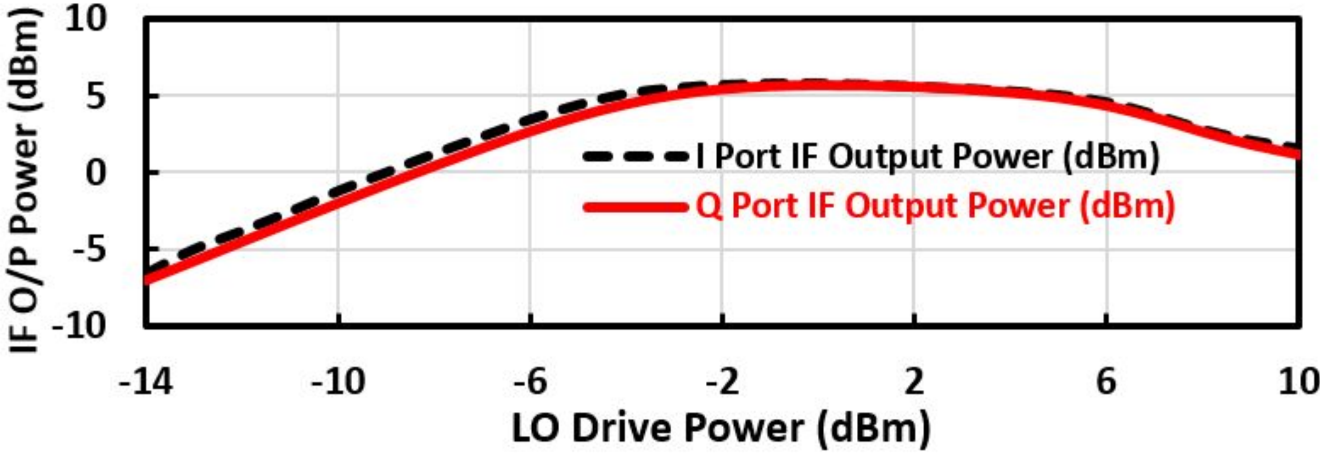
- The I/Q demodulator

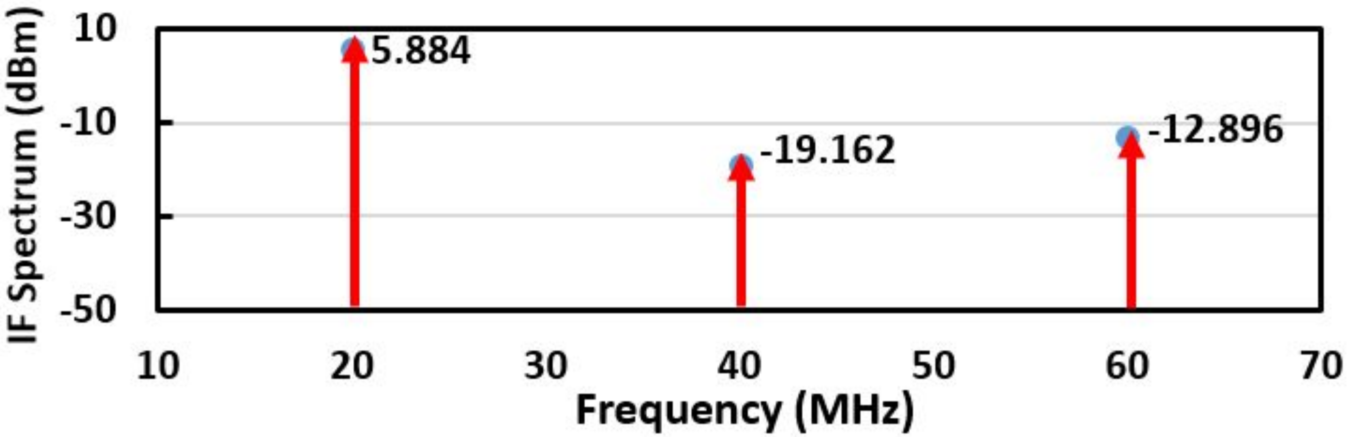
1. The active area equals 0.22 mm^2.
2. The total area including the pads is 0.6 mm^2.



Post –layout Simulation Results

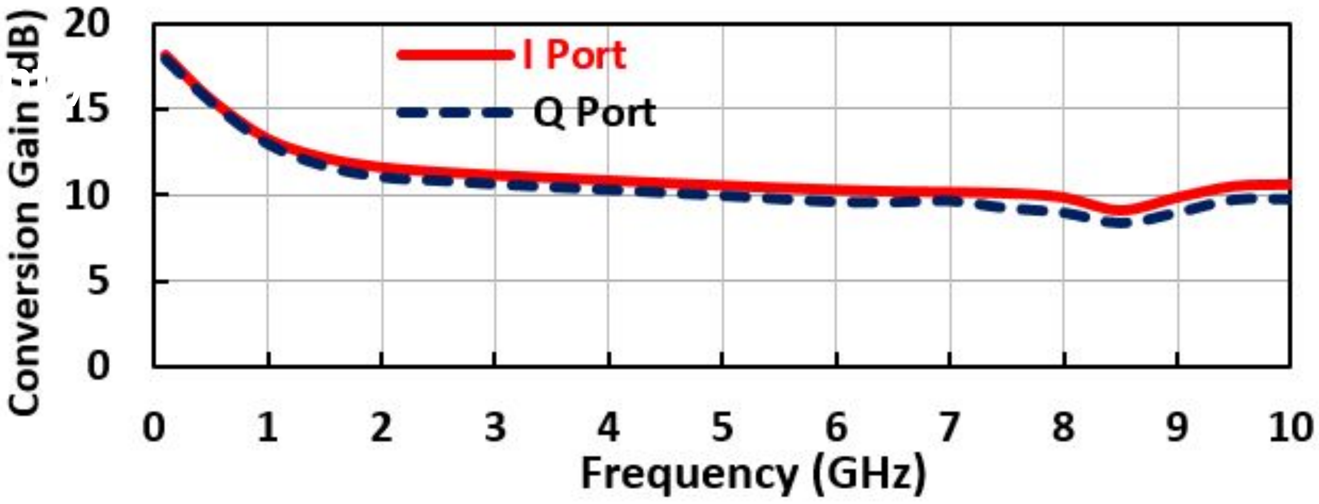
- The IF output power is simulated versus LO power. At RF frequency =4.48 GHz and LO frequency =4.5 GHz.
- The optimum LO power is chosen to be 0 dBm.
- The output spectrum has a fundamental power of 5.884 dBm at 20 MHz, while the second, and the third harmonics power equal -19.2 and -12.9 dBm at 40 and 60 MHz, respectively.

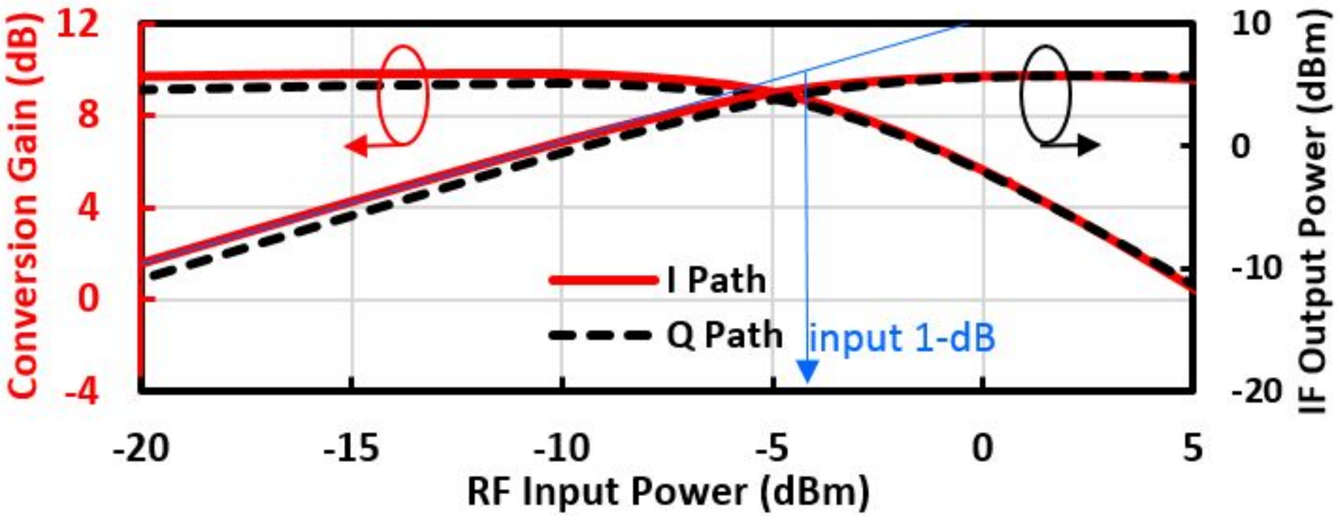




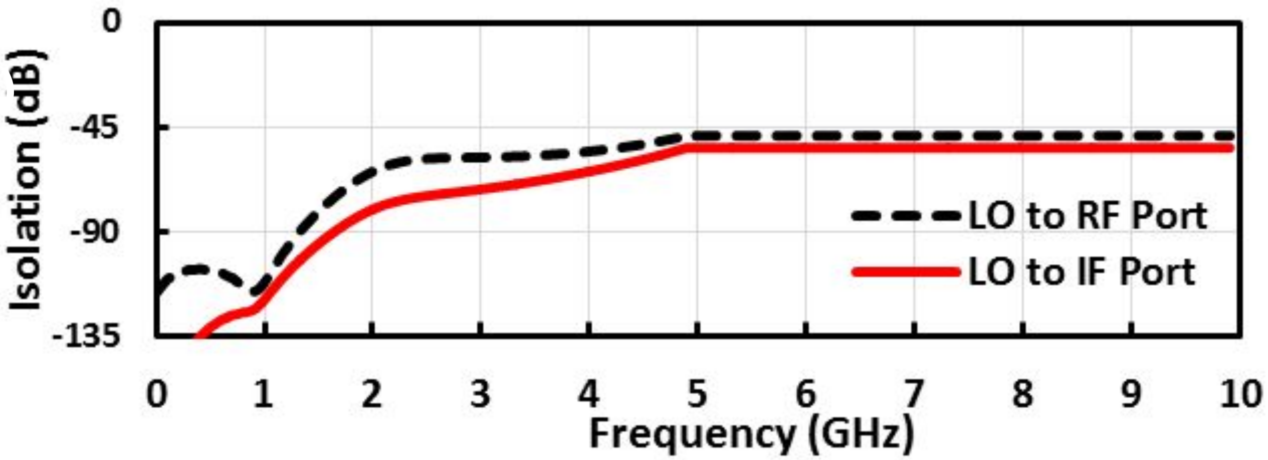
Post –layout Simulation Results (co

- I and Q ports conversion gain versus frequency.
- The simulated CG is greater than 10 dB in the frequency range from 0 to 10 GHz.
- The I/Q mismatches do not exceed ± 0.3dB, in general the I/Q mismatches are generated due to the variations of layout design rules, also the trace lengths of I+, I-, Q+, Q- are not perfectly identical.
- The simulated input 1-dB compression point is -4.15 dBm, at RF frequency of 4.48 GHz and LO frequency equals 4.5 GHz .

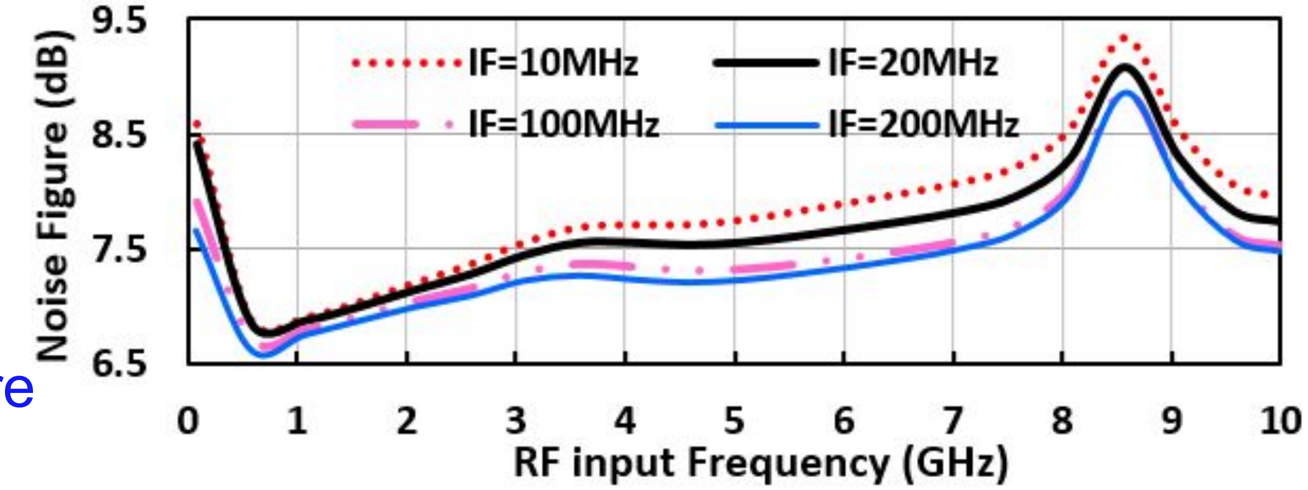




Post –layout Simulation Results (cont.)



- LO to RF port isolation, and the LO to IF port isolation versus frequency.
- The LO to RF port and LO to IF port isolations are less than -45 dB in the frequency range from 0 to 10 GHz.



- The simulated SSB noise figure with RF input frequency at different values of IF frequencies.
- The minimum value of the SSB noise figure is 6.55 dB when IF frequency equals 200 MHz.

Index	**This work**	**[16]** Journal of Semiconductors (**2015**)	**[17]** IEEE Transactions on Circuits and Systems II(**2014**)	**[18]** Prime Asia Conference (**2017**)	**[19]** ETRI Journal (**2018**)
Function	I/Q demodulator (low noise I/Q demodulator)	I/Q mixer	LNA+ mixer	LNA+IQ Mixer	Receiver (low noise I/Q demodulator)
Freq. (GHz)	0-10	10.25-13.75	2.4	2.4	0.48-0.7
Process (nm)	130	65	130	180	130
CG (dB)	10 *	7-8 **	25 **	22 **	48 **
			NA		
NF(dB) SSB		11.3	3.5 DSB	9.16	4.8
PDC(mw)	10.5	7.2	3.6	6.3	42-88
Supply (V)	1.2	1.2	1.2	1.8	1.5/2.5
Area (mm2) Active area	0.22	0.55 chip area	0.4	1.232 chip area	NA
Results	Post Layout Simulation	Measured	Measured	Simulation	Measured

***Power conversion gain is ratio between output power to input power**

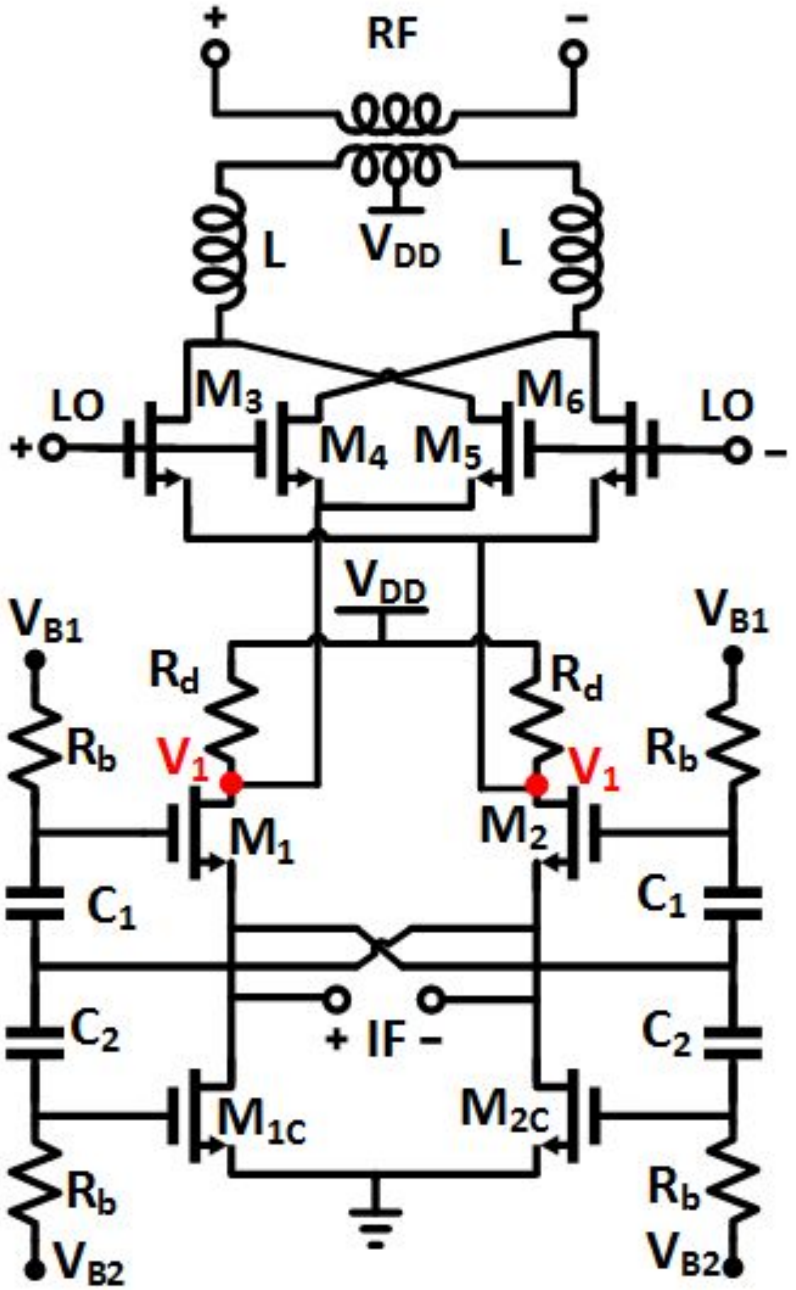
****Voltage conversion gain is ratio between output voltage to input voltage**

3

Proposed Wideband Modulator

Proposed Wideband Up-Conversion Mixer

- The IF transconductance stage is a CCC common gate configuration to achieve good IF matching with high conversion gain, low power dissipation, and save the die area at the expense of the circuit complexity.
- The local oscillator (LO) switching transistors M_3–M_6, to perform frequency translation.
- The RF output port is wideband matched by means of a five-ports transformer with a series peaking technique to extend bandwidth.

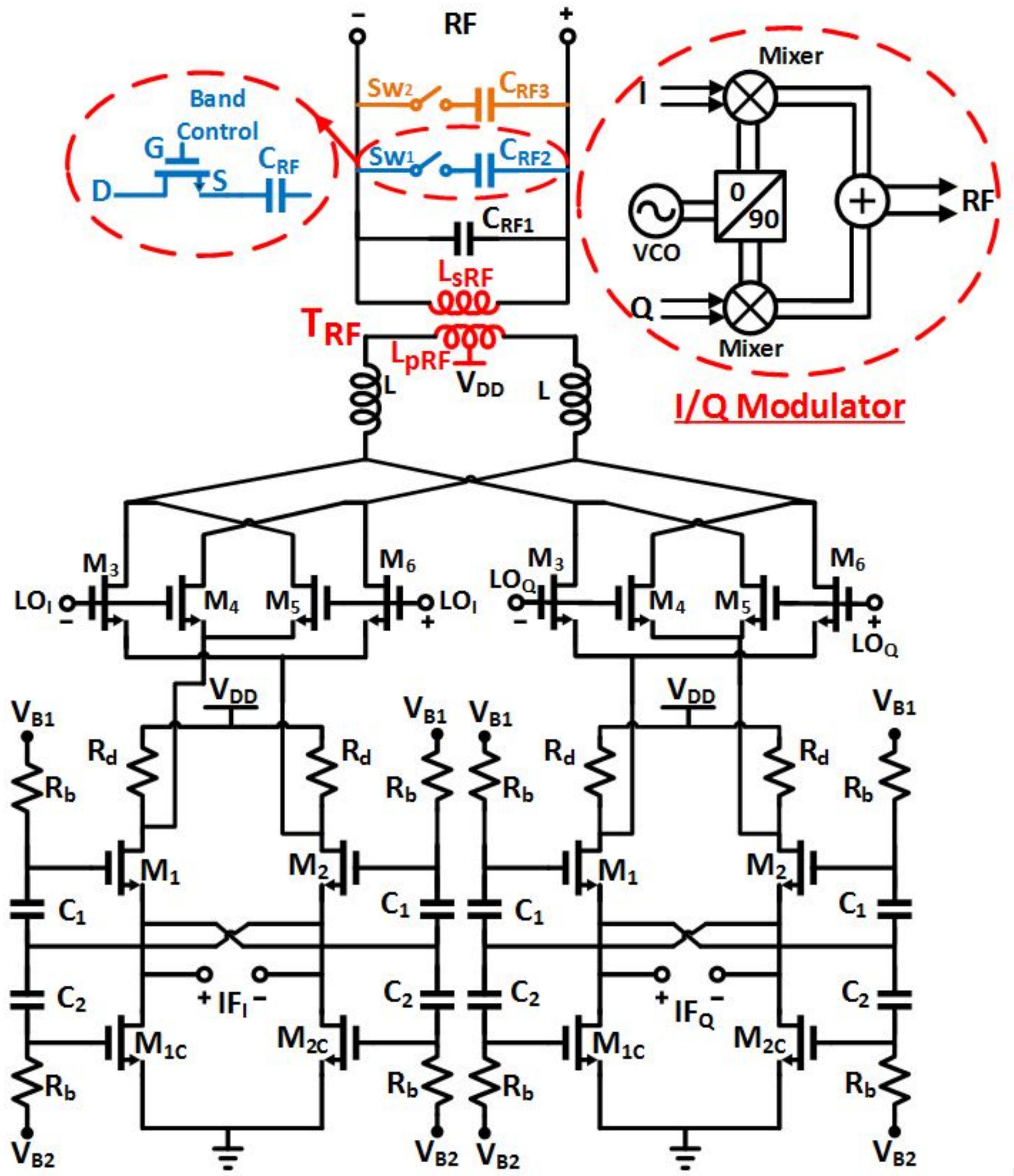


Proposed CMOS I/Q Modulator

- The modulator consists of:

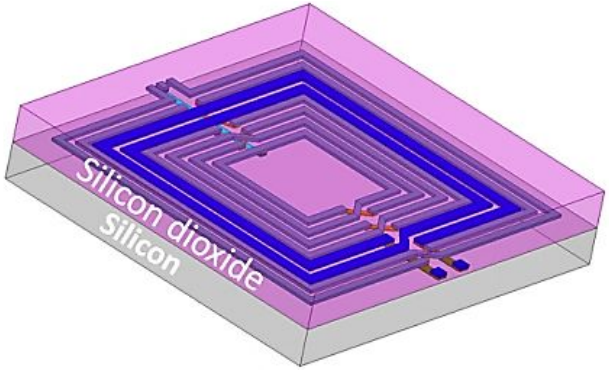
1. CCC common gate stages,
2. Two up-conversion mixers,
3. The 5-ports transformer along with switched capacitors bank for reconfigurable RF output matching.

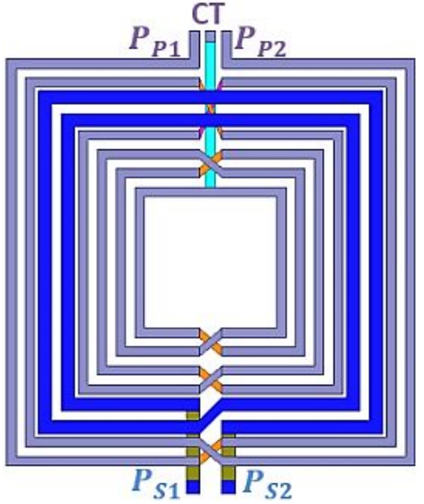
- The high coupling factor wideband 5-ports transformer that achieves wide output matching consists of a symmetric center tapped primary inductor and a spiral secondary inductor.
- The primary and secondary winding are designed in top metal (M8) to reduce series resistance and capacitance to substrate.

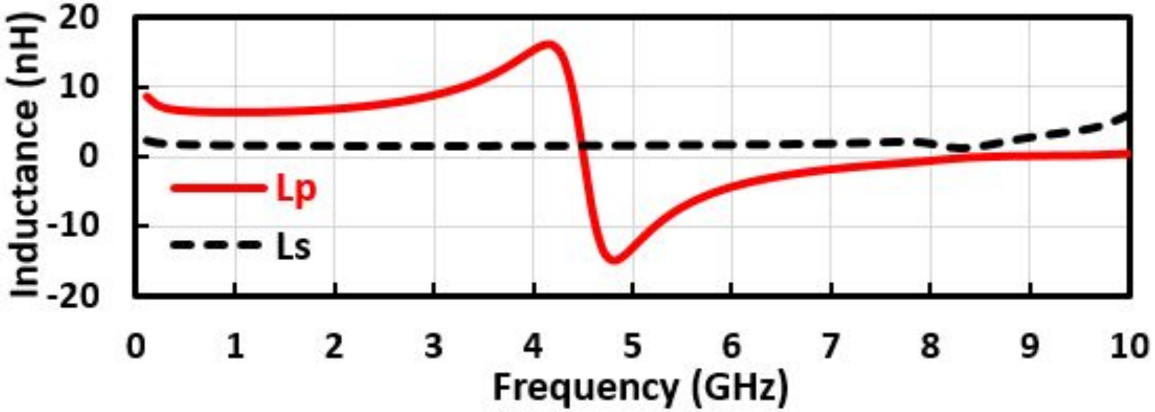


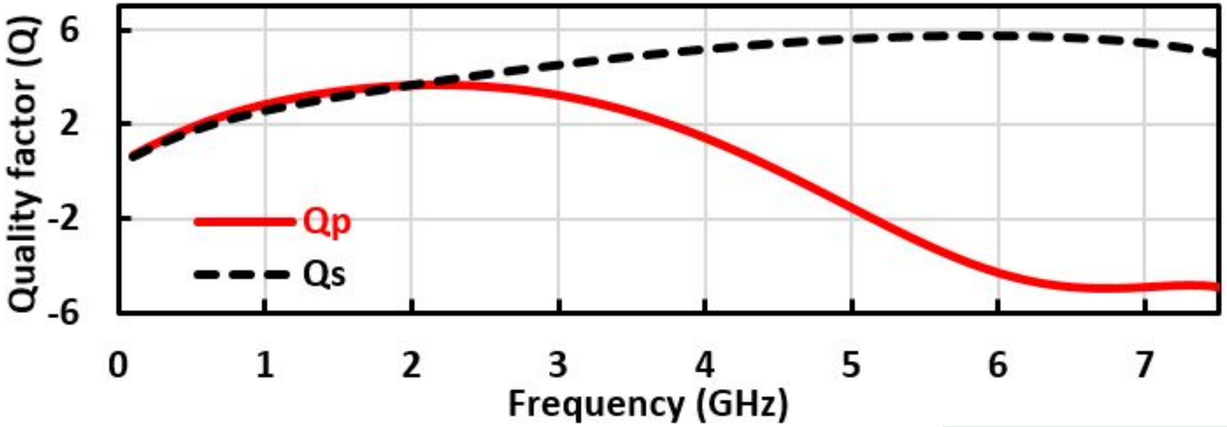
Proposed 5-ports transformer

- The primary and the secondary inductors have 6 and 2 turns respectively leading to an effective turns ratio of approximately 4.24.
- The proposed transformer has a primary inductance of $L_P = 6.4$ nH, secondary inductance of $L_S = 1.5$ nH, self-resonance frequency (SRF) of the primary and secondary inductors of 4.6 and 15 GHz respectively.
- The coupling coefficient of the proposed transformer is $k = 0.8$, and the quality factor of primary and secondary inductors is $Q_p = 4$, and $Q_S = 6$, respectively.





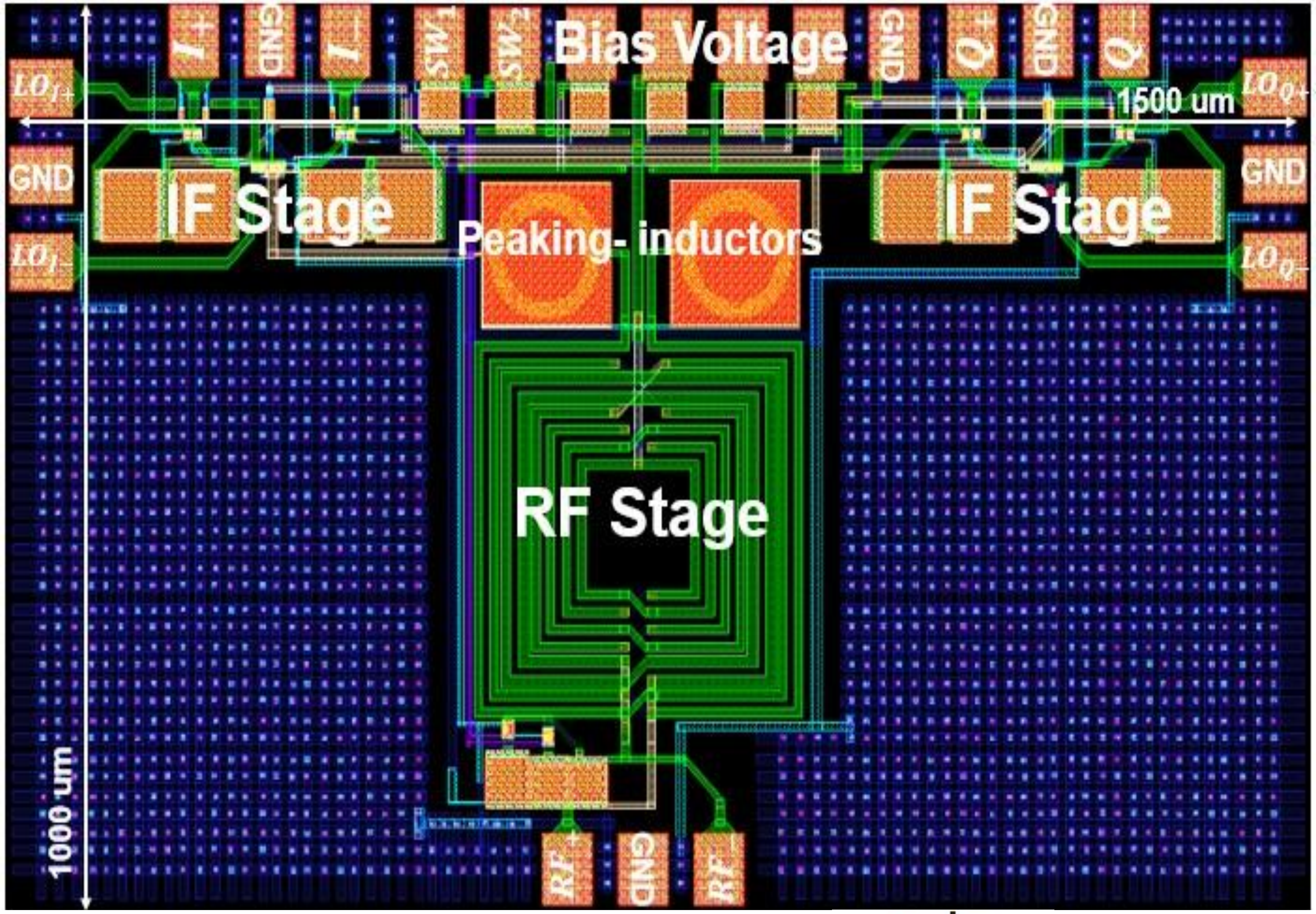




I/Q Modulator Layout

- The layout of the proposed I/Q modulator.

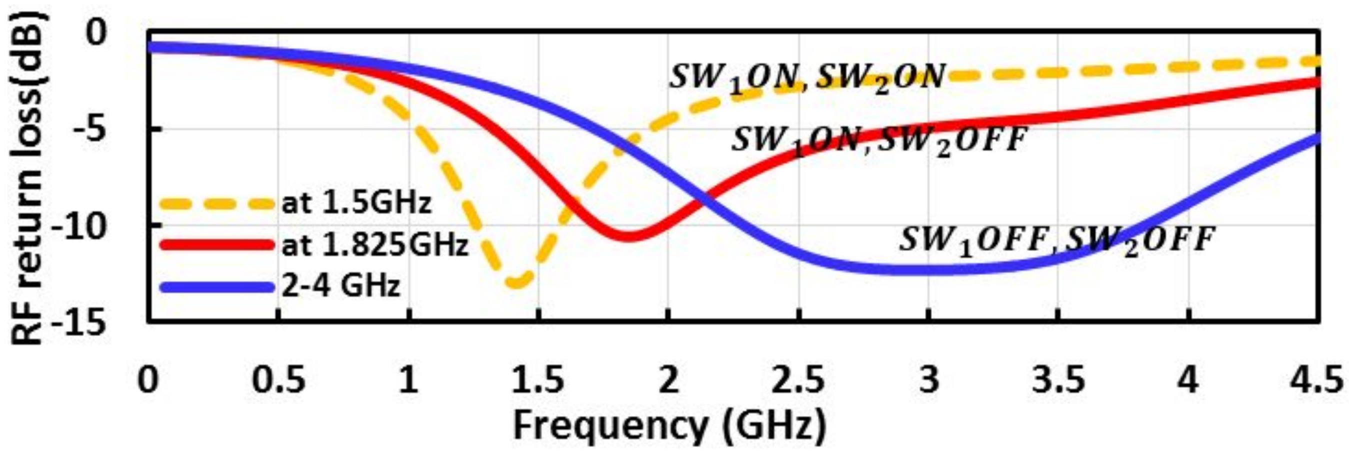
1. The active area equals $0.55\ mm^2$.
2. The total area including pads is $1.5\ mm^2$.



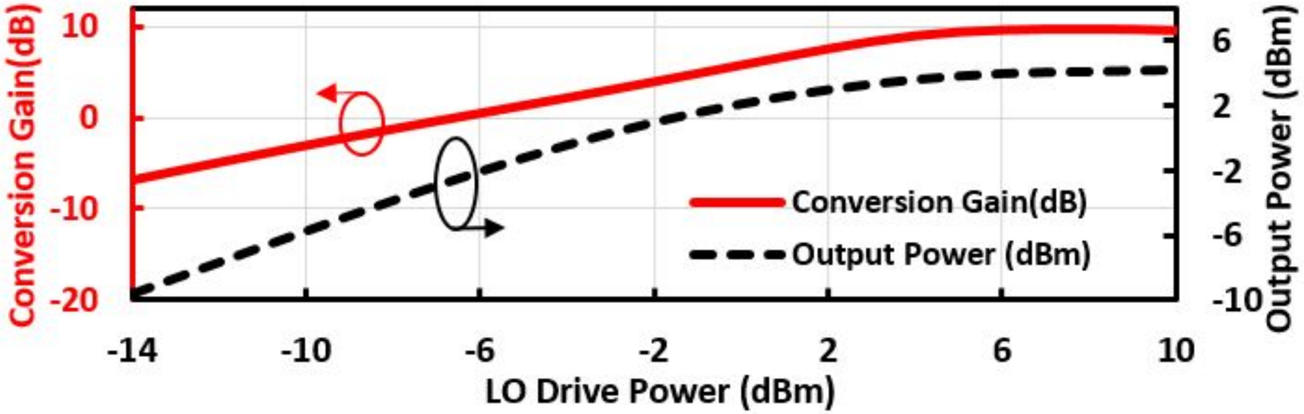
I/Q Modulator Post –layout Simulation Results

- The RF output matching of the proposed I/Q modulator is reconfigurable by switching the capacitors $C_{RF2,3}$.
- The switches are implemented by NMOS transistors and controlled by the gate voltage where OFF switch means zero gate voltage and ON means VDD on the gate of the transistor.
- The selection of the bands are based on the states of the switches $Sw_1, and\ Sw_2$ as illustrated in the table.
- The RF output return loss covers the frequency band from 1.2 to 4 GHz.

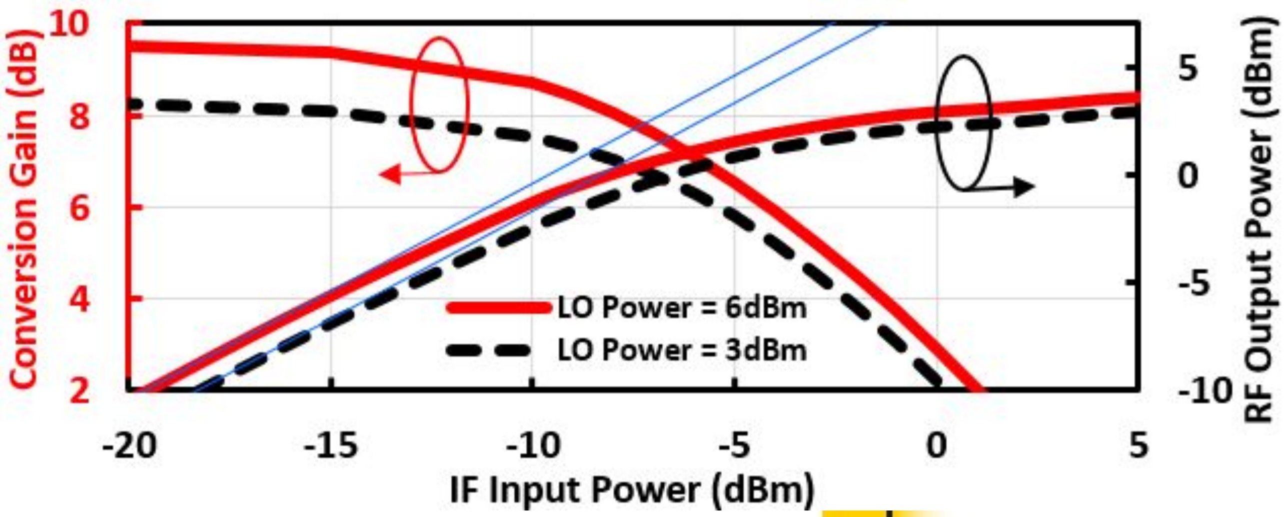
SW1	SW2	Covered Frequency band
OFF	OFF	2.1 to 4 GHz
ON	OFF	1.6 to 2.2 GHz
ON	ON	1.2 to 1.6 GHz



- The conversion gain and output power versus LO power at 2.5 GHz.
- By applying 3 dBm in the LO power, the maximum conversion gain achieved is 8.32 dB, and the output power is 3.4 dBm.

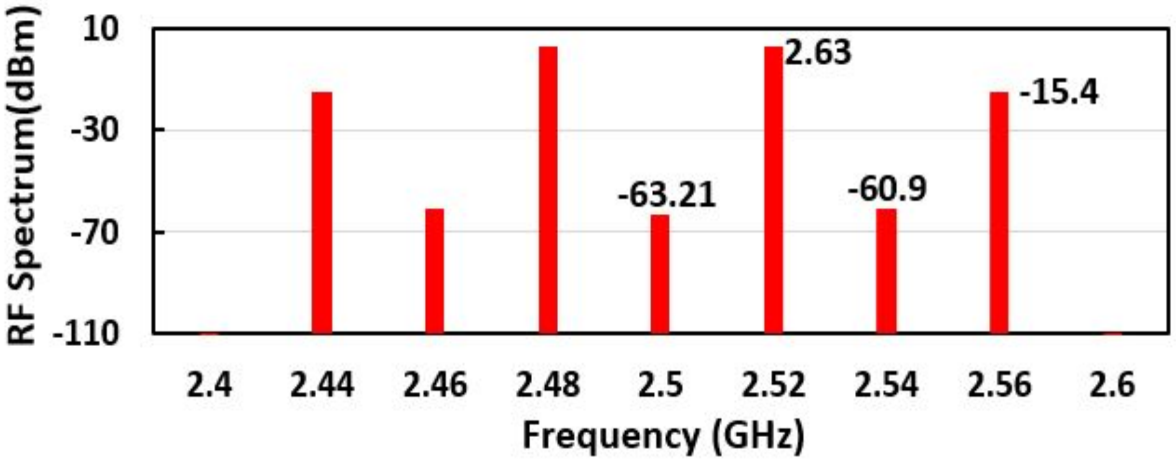


- The CG, and RF output power are simulated against IF input power, at different values of the LO power.
- The output 1-dB compression point (OP_{1dB}) is -1.6 dBm at the LO power of 3-dBm.
- In accordance with rising the LO power from 3 to 6 dBm, OP_{1dB} will be improved from -1.6 to -0.9 dBm.
- The proposed modulator can be applied to high output power and high linearity systems with increased LO power.

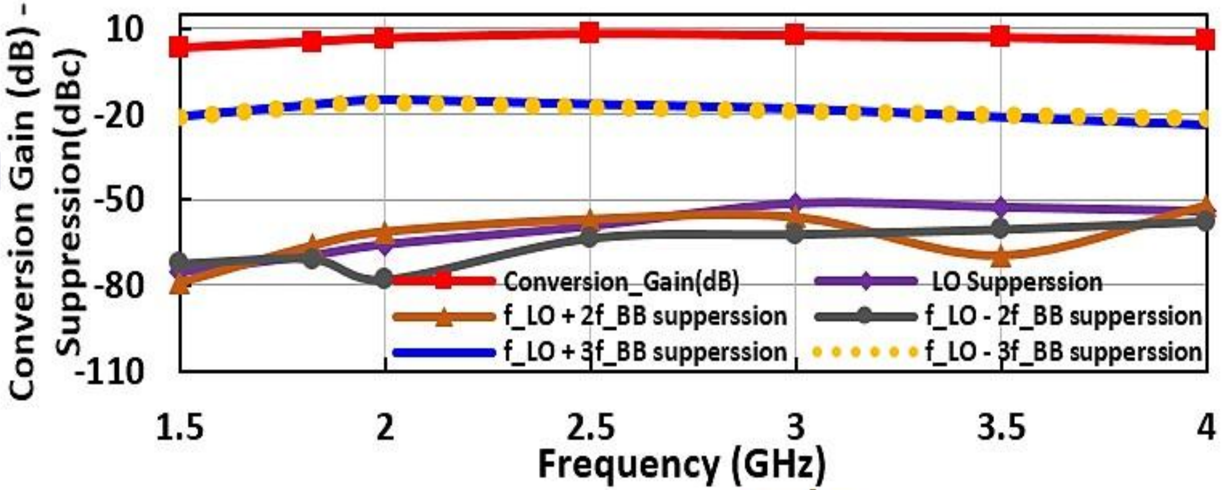


I/Q Modulator Post –layout Simulation Results (co

- The output spectrum of the proposed I/Q modulator has RF frequency of 2.48/2.52 GHz, an LO frequency of 2.5 GHz, and baseband frequency of 20 MHz.
- The spectrum contains the LSB and the USB.



- The simulation results of the conversion gain, LO suppression, and harmonic suppression from 1.5 to 4 GHz.
- The modulator demonstrates excellent conversion gain (CG) flatness of 8.4 dB in the frequency band from 1.5 to 4 GHz.
- The simulated LO suppression is better than -60 dBc from 1.5 to 4 GHz. The simulated harmonic suppression, $f_{LO} \pm 2f_{BB}$ and $f_{LO} \pm 3f_{BB}$ of the modulator are better than -50 dBc from 1.5 to 4 GHz.



COMPARISON WITH THE STATE-OF-THE ART

Index	This work	[14] Journal of Semiconductors (2014)	[15] IEEE Journal of Solid-State Circuits (2019)
Function	I/Q modulator	Up-Conversion I/Q Mixer	I/Q modulator
Freq. (GHz)	1.5 - 4	2.4-2.48	DC-60
Process (nm)	130	180	45 SOI
CG (dB)	8.4 *	5 *	NA
NF(dB) SSB	-------	-------	--------
PDC(mw)	16.6	1.4	200
Supply(V)	1.2	1	3
Area(mm2) Active area	0.55	0.507	0.018
Results	Post Layout Simulation	Measured	Measured

*Power conversion gain is ratio between output power to input power

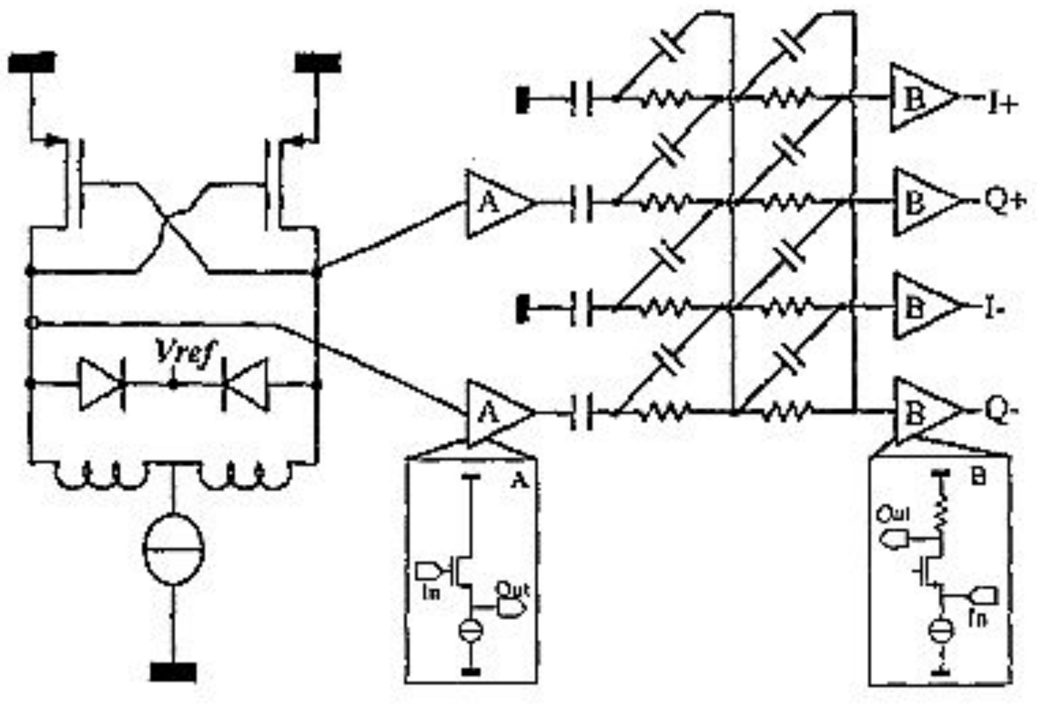
**Voltage conversion gain is ratio between output voltage to input voltage

4

Proposed Quadrature Voltage Controlled Power Oscillator

Previous work

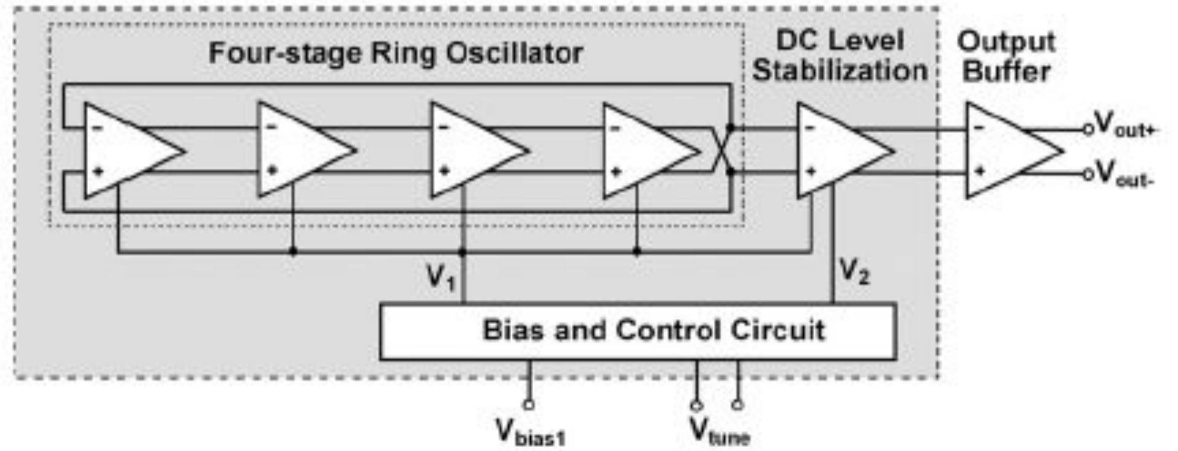
- Quadrature phases can be generated using many techniques such as
- RC poly-phase filter [20], the cascaded RC filter stages are wanted to produce good quadrature signals, and this attenuates the signal significantly and perhaps must be buffered from the preceding VCO.



[20] M. Borremans, B. De Muer and M. Steyaert, "The optimization of GHz integrated CMOS quadrature VCO's based on a poly-phase filter loaded differential oscillator," **2000 IEEE International Symposium on Circuits and Systems (ISCAS),** Geneva, Switzerland, 2000, pp. 729-732 vol.2.

Previous work cont.

- Another method is the ring oscillators [21], the ring oscillator consumes less area than an LC VCO, but they have poor phase noise, and consume high power. So that the ring oscillators are disqualified in modern RF transceivers application.



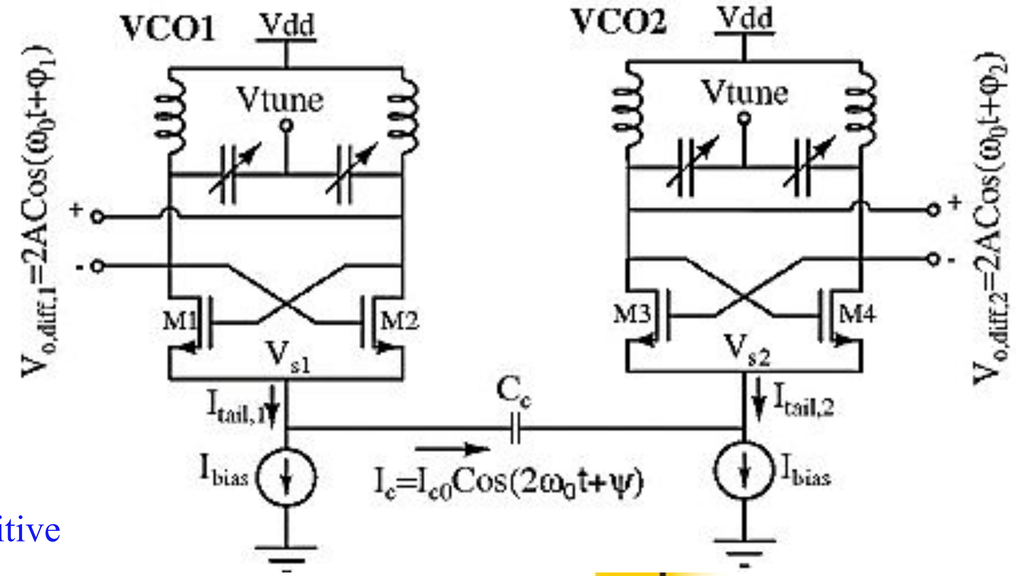
[21] C. S. Azqueta, S. Celma, and F. Aznar, "A 0.18μm CMOS ring VCO for clock and data recovery applications," **Microelectronics Reliability**, no. 51, pp. 2351–2356**, 2011**.

- quadrature voltage-controlled oscillators (QVCO), usually minimize the power consumption at the expense of silicon area.

Conventional QVCO consists of two similar cross coupled LC oscillators, where the LC oscillators couple through passive elements, and it is called passive coupling [22]

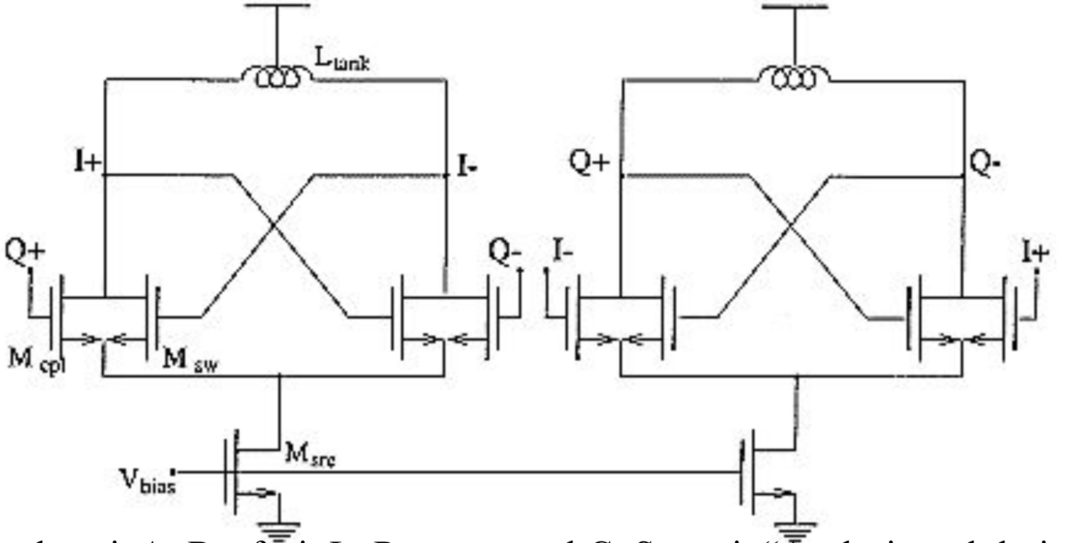
The passive coupling quadrature VCOs demonstrate good phase noise, but have a significant I/Q phase error.

[22] B. Soltanian and P. Kinget, "A low phase noise quadrature LC-VCO using capacitive common-source coupling," in Eur. **Solid-State Circuits Conf., Sep. 2006**, pp. 436–439.

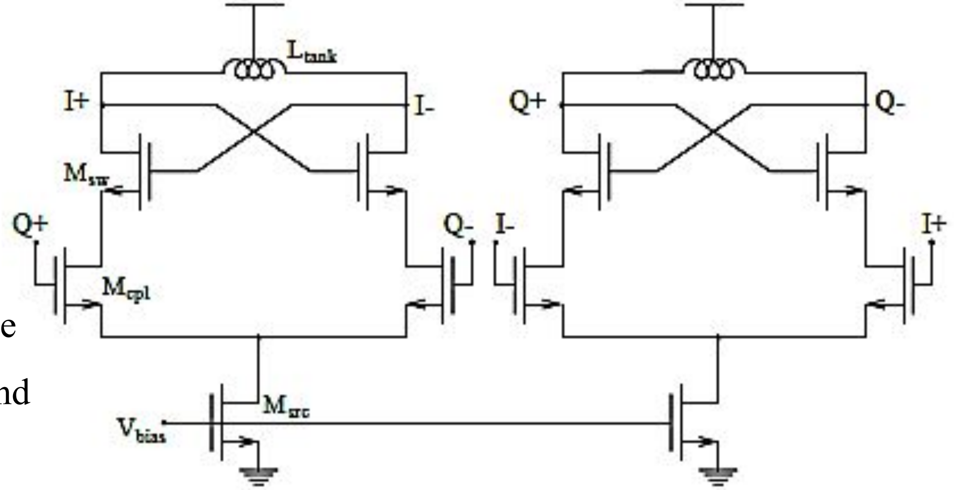


Previous work cont.

- through active devices, called active coupling. In contrast, the active coupling quadrature VCOs are strong enough to suppress the quadrature phase error. Also, the active coupling can be achieved either in
- parallel QVCO (P-QVCO) [23] or
- in series QVCO (S-QVCO) [24]. The phase noise and phase error trade-off is very strong in the P-QVCO, and much less in S-QVCO.



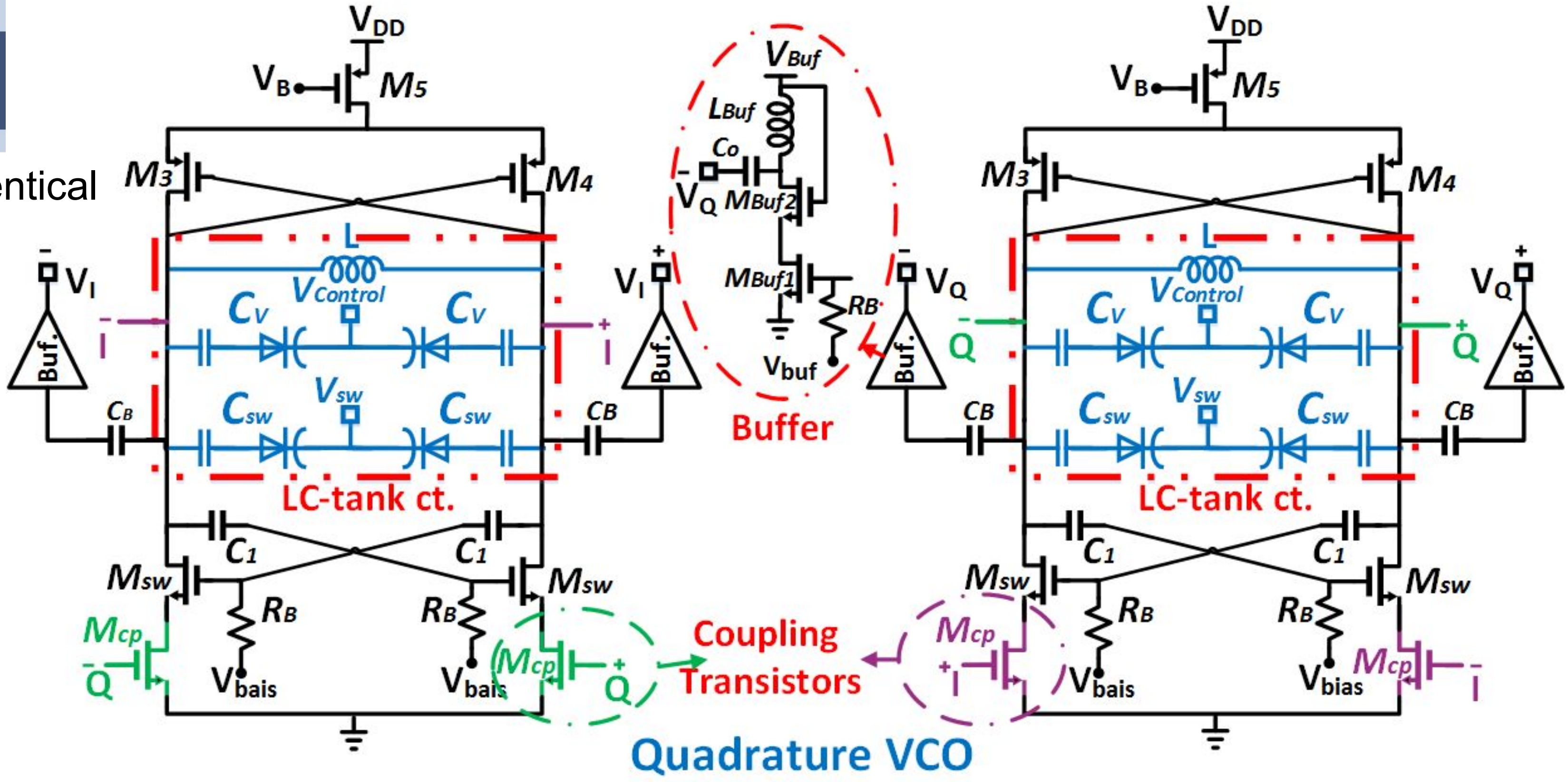
[23]P. Andreani, A. Bonfani, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," **IEEE J. Solid-State Circuits**, vol. 37, no. 12, pp. 1737–1747, **Dec. 2002**.



[24] P. Andreani , "A 2 GHz, 17% tuning range quadrature CMOS VCO with high figure-of-merit and 0.6 phase error," in Proc. ESSCIRC, Sept. 2002.

Proposed QVCO

- The proposed QVCO consists of two identical cross coupled LC-oscillators.
- The proposed LC VCO consists of
1. Cross-coupled NMOS pair (Msw),
2. Cross-coupled PMOS pair (M3-M4),
3. PMOS current source (M5),
4. Improved varactor capacitor (Cv) for frequency tuning,
5. Enhanced switching capacitor (Csw) to operate in two bands,
6. High Quality-factor inductor (L) .



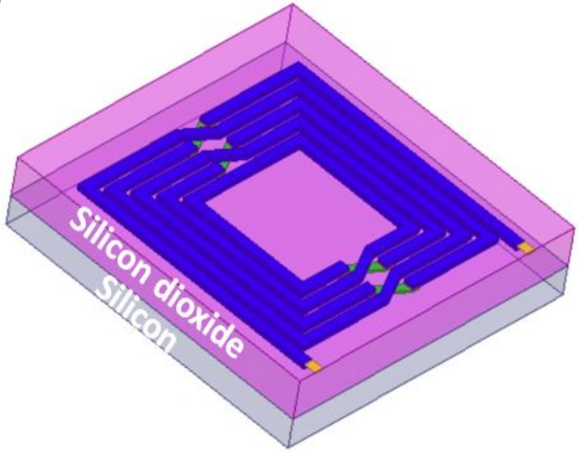
- The improved varactor consists of MOS varactor series with MIM capacitor to improve the phase noise.
- The oscillation frequency of VCO is determined using the following equation: $f_{osc} = \frac{1}{2\pi\sqrt{L*0.5*(C_V+C_{sw}+C_{par})}}$
- Where Cpar is the parasitic capacitance of the VCO core output node and the buffer input capacitance.
- As the name series coupling quadrature VCO suggests, the coupling transistors are connected in series with the switching transistors.
- There are four output buffers, each buffer consists of two NMOS, and series inductor connected as cascode amplifier to increase the voltage swing, and maximize the output power.

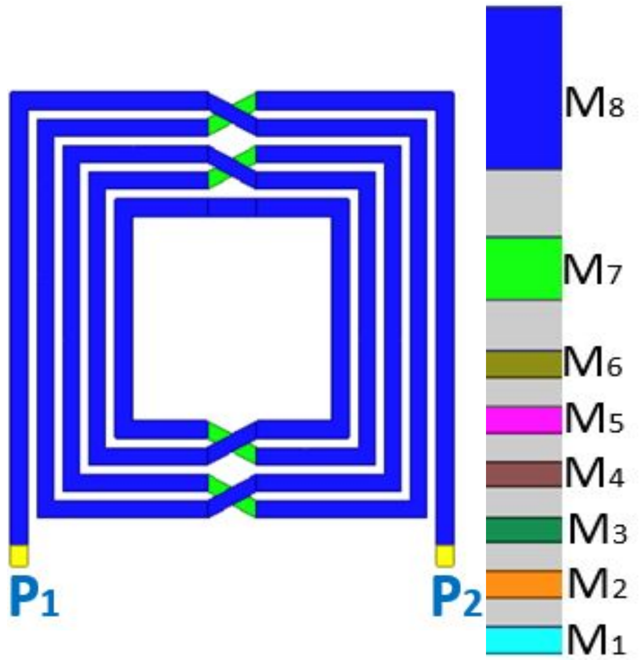
Proposed LC-tank

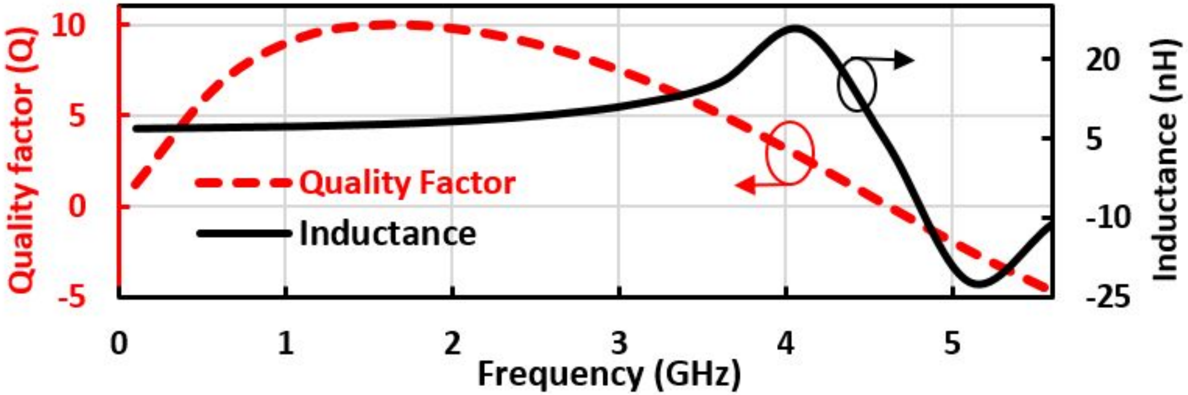
- The proposed LC-tank circuit consists of proposed inductor, improved switching varactor to achieve dual bands and tuning varactor to tune between the minimum and maximum oscillation frequencies .
- The proposed inductor is designed using the two top metal layers (M8 and M7) in umc130nm technology and simulated using High-Frequency Structure Simulator (HFSS) to ensure accurate results then the s-parameters of the inductor are inserted in the proposed QVCO design to have post-layout simulation results.

Proposed LC-tank (cont.)

- The number of turns in the proposed inductor equals five
- The inductor was designed to achieve maximum Q-factor, high self-resonance frequency and compact size.
- The proposed inductor has inductance of 9 nH, Q = 10, and self-resonance frequency equals 4.8 GHz





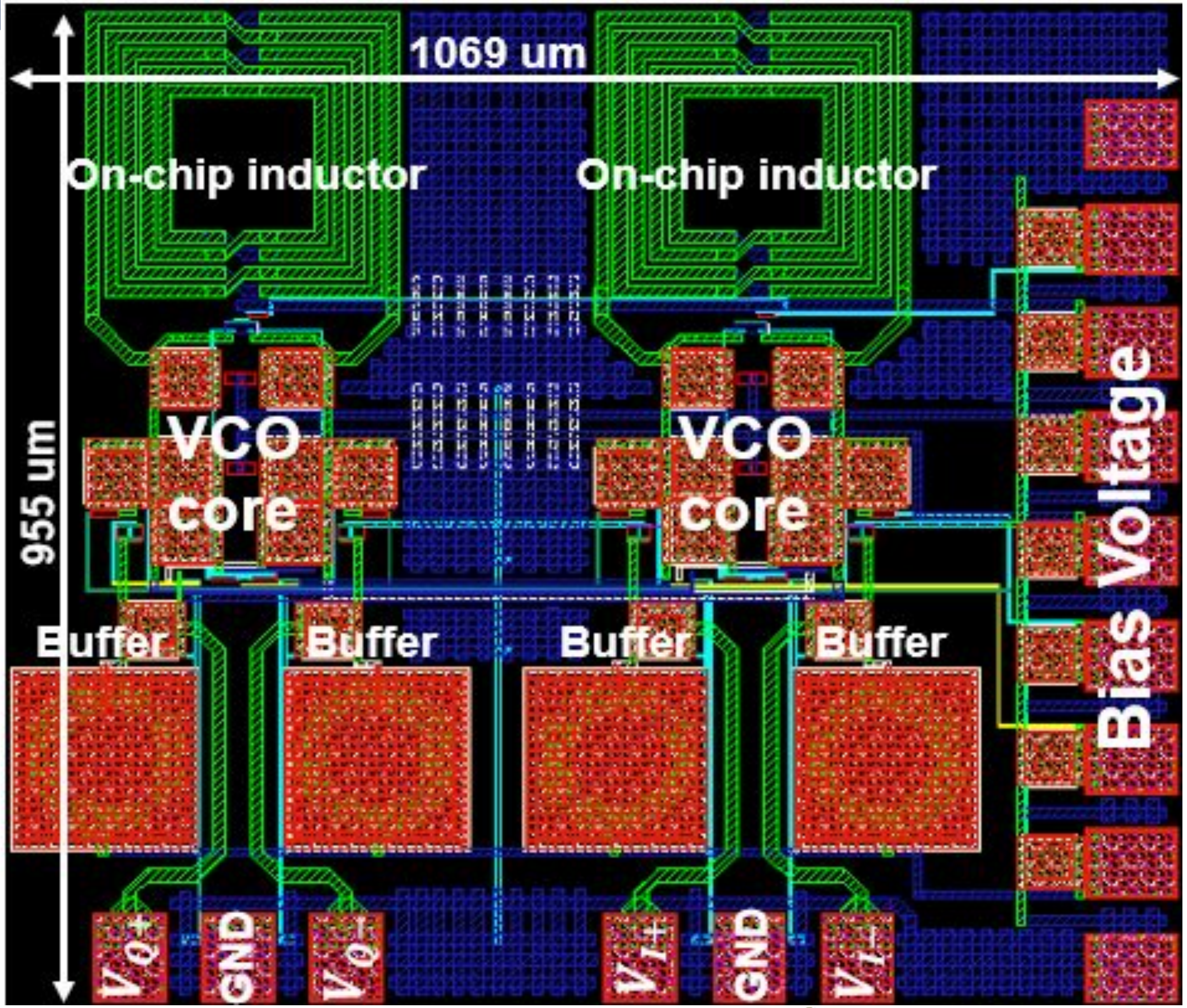


Parameters	Inductance	Maximum Q-factor	Self-Resonance Frequency	Dimension µm2
Proposed inductor	9 nH	10	4.8 GHz	289 * 289

QVCO Layout

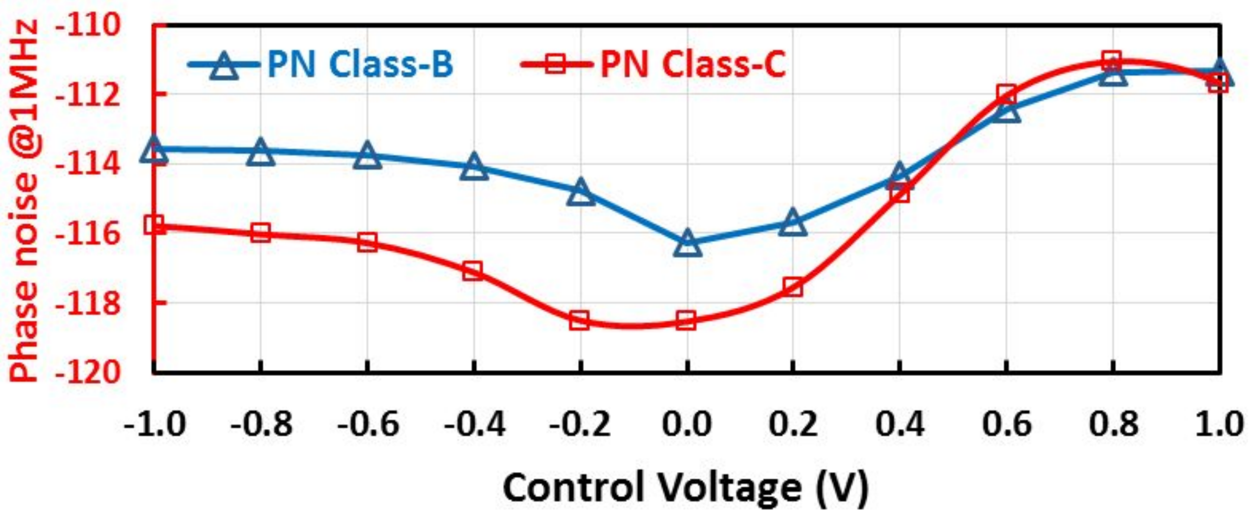
- The proposed QVCO

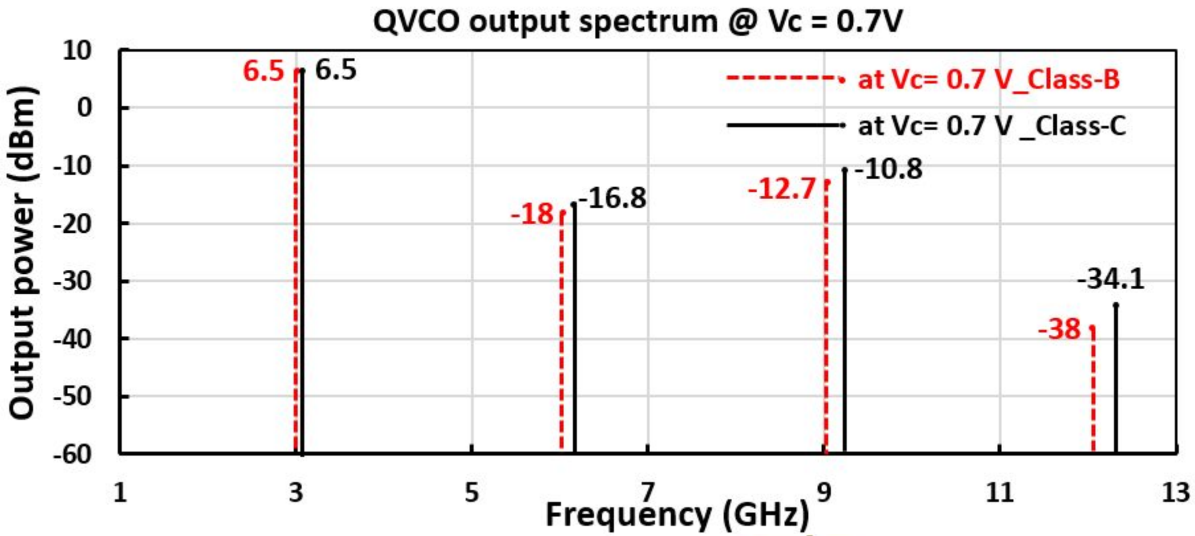
1. Active area equals 0.34 mm^2,
2. The total area included four output buffers, and pads is 1 mm^2.



Post –layout Simulation Results

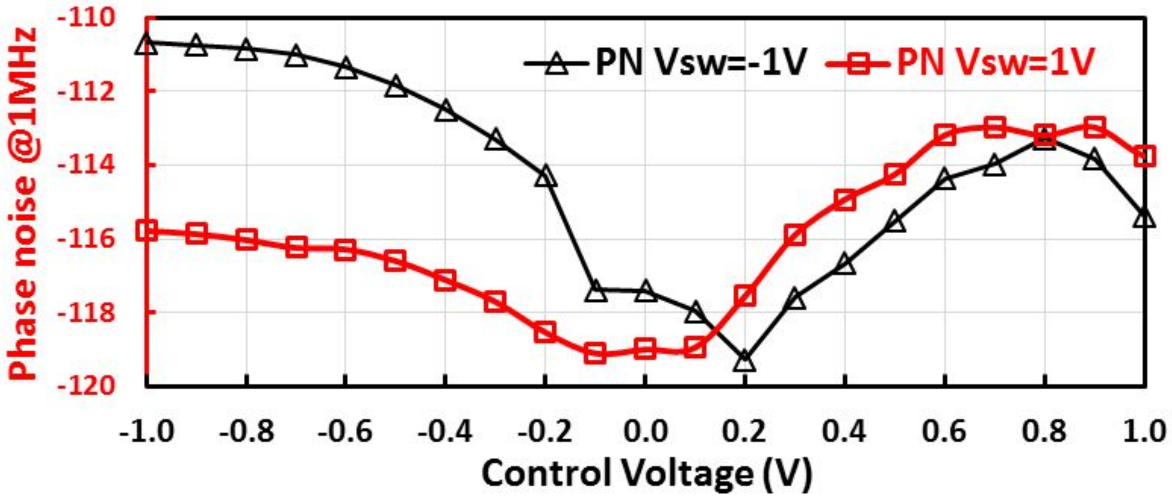
- The phase noise at 1 MHz offset of the proposed QVCO at class-B bias, and class-C bias.
- The phase noise at class-C bias is improved by 2 to 3dB compared to class-B bias.
- The proposed QVCO output spectrum at control voltage equals 0.7V.
- The class-B operation has lower harmonics amplitude than class-C operation.

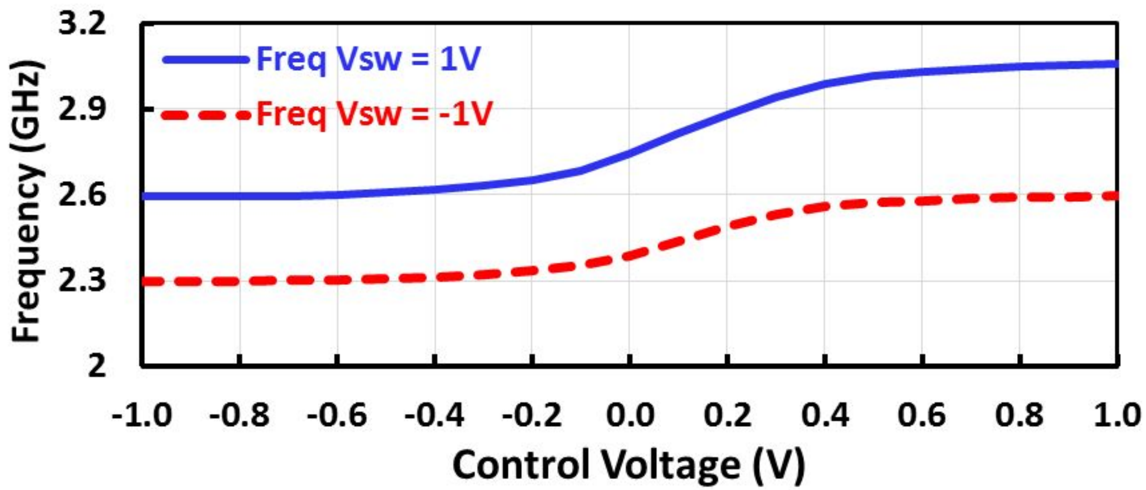




Class-C Operation

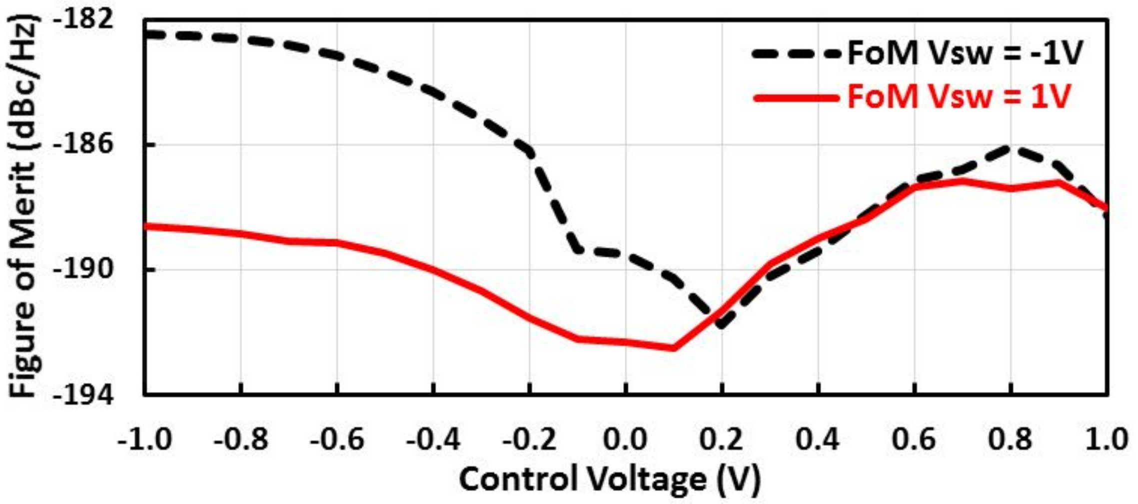
- Class-C operation is achieved when the switching transistors are biased with $V_{bias} = 0.36V$.
- The phase noise of the proposed Class-C QVCO at 1 MHz offset changes from -111 to -119.3 dBc/Hz.
- The proposed Class-C QVCO has frequency tuning range (FTR) of 28.2 % from 2.3 to 3.1 GHz.



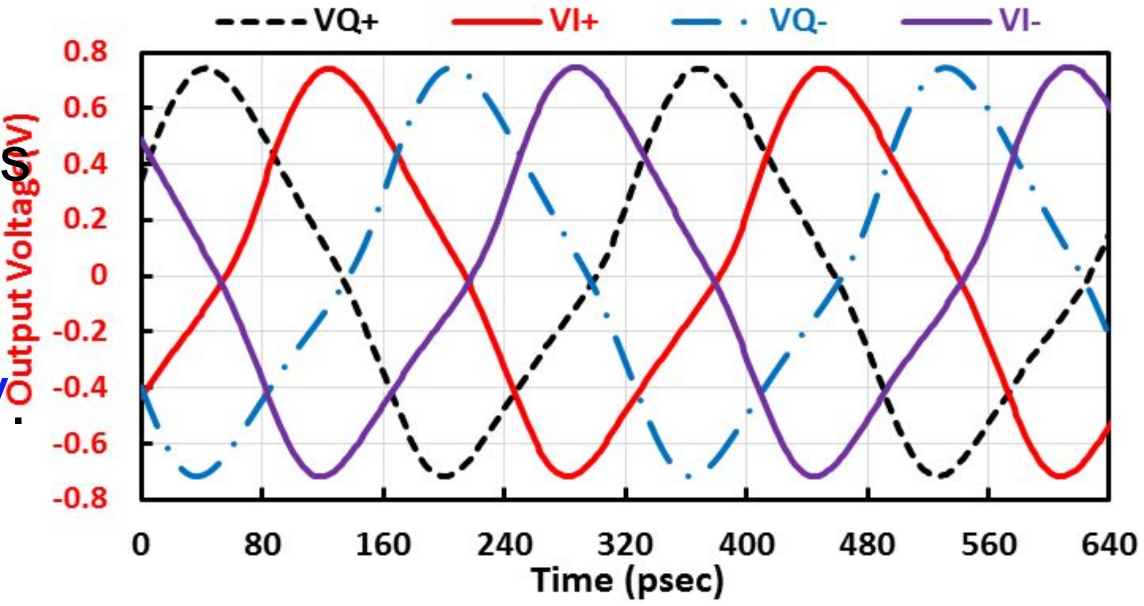


Class-C Operation (cont.)

- The simulated figure of merit (FoM) of the proposed Class-C QVCO versus control voltage.



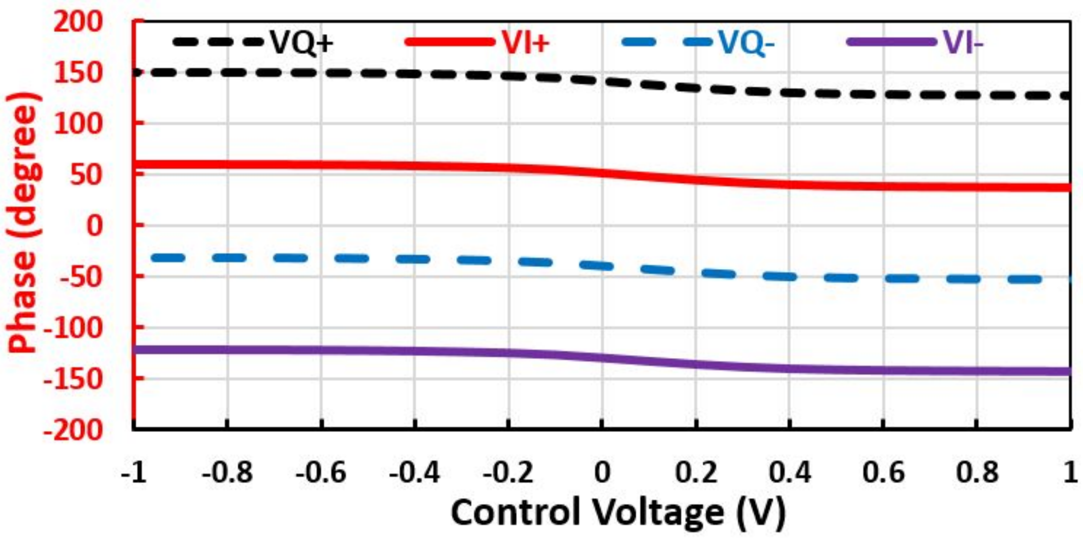
- The minimum value figure of merit is -192 dBc/Hz.
- The time domain of quadrature output signals for the proposed Class-C QVCO.

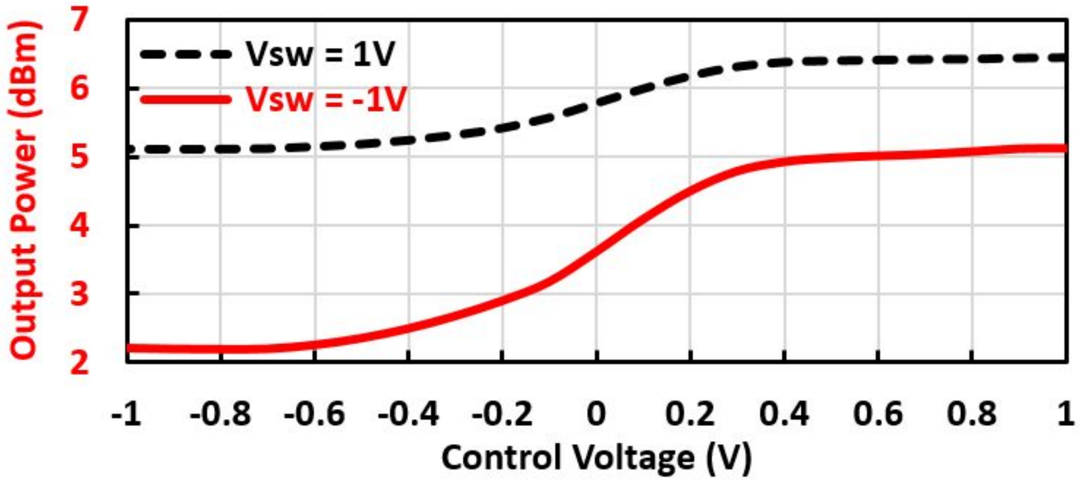


- The peak to peak output signal equals 1.5 V.

Class-C Operation (cont.)

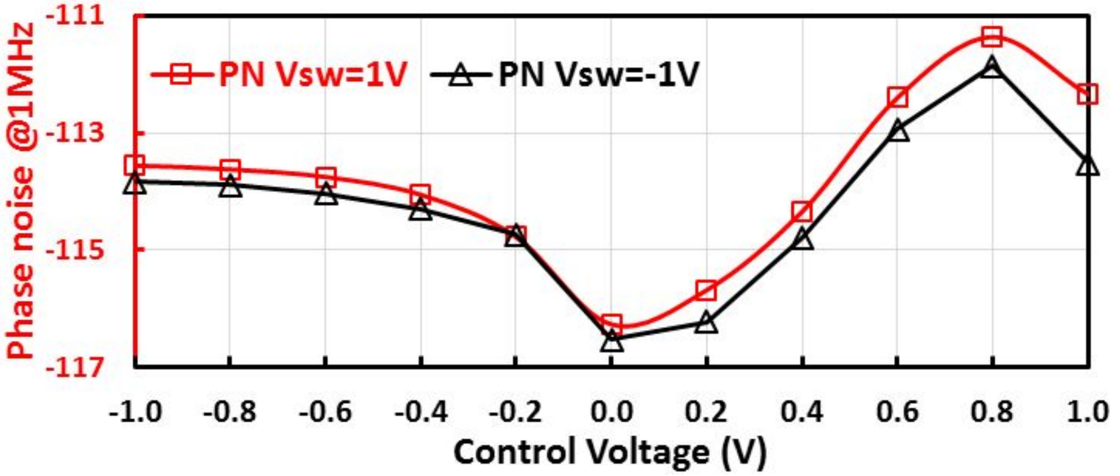
- The phase of quadrature output signals for the proposed Class-C QVCO versus control voltage.
- The phase error between the output signals equals $\pm 0.25^{\circ}$.
- The dBm output power of the proposed Class-C QVCO with control voltage .
- The output power in range between 2.25 to 6.5 dBm, the maximum dBm value is 6.5dBm.



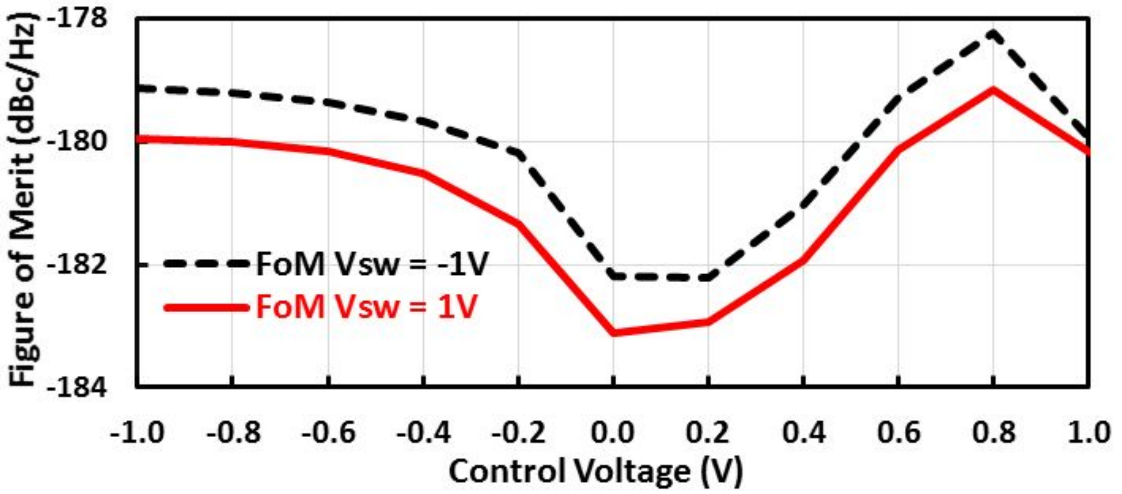


Class-B Operation

- Class-B operation is achieved when the switching transistors are biased with $V_{bias} = 0.5V$ and has phase noise at 1 MHz offset of -111.3 to -116.5 dBc/Hz.



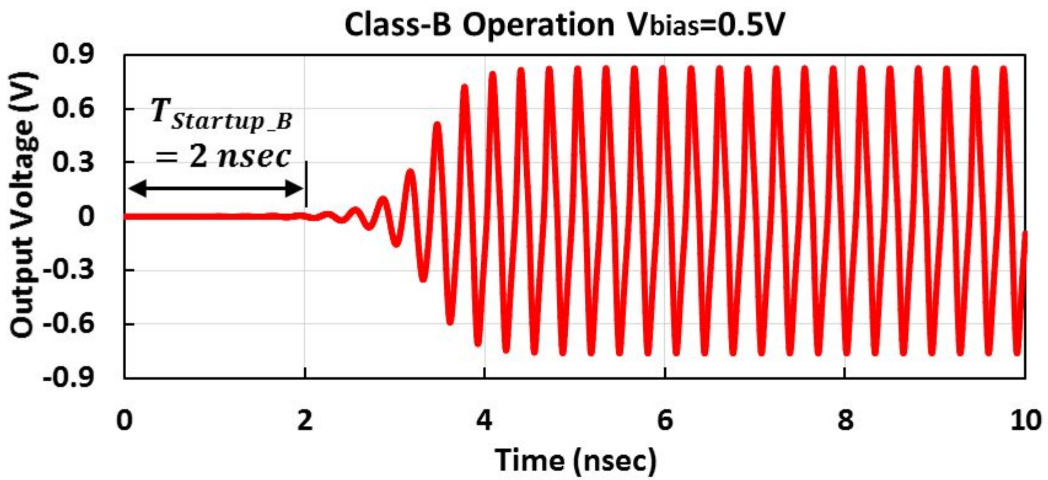
- The simulated figure of merit (FoM) versus control voltage, the minimum value is -183 dBc/Hz.

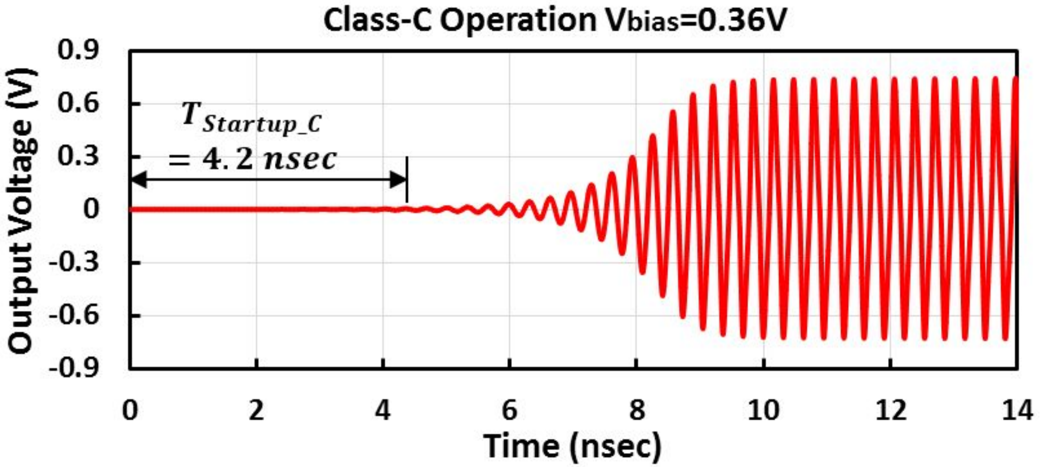


- The frequency tuning range equals 28.5% from 2.25 to 3.001 GHz, and the peak to peak output voltage signal equals 1.65V. The maximum output power equals 6.8 dBm, and Class-B QVCO consumes 1.48 mW power from 1 V supply voltage.

The start-up time of the proposed Class-C/B Q

- The start-up behaviour and the maximum oscillation amplitude of the proposed QVCO.
- For class-B operation, the start-up time is 2 nsec and peak amplitude of 821mV at 3GHz oscillation frequency.
- For class-C operation, the start-up time is 4.2 nsec and it has maximum amplitude of 750mV when the oscillation frequency equals 3GHz.





Parameters		PN (dBc/Hz)	Start-up Time (nsec)	Max. oscillation amplitude (V)
Class-C	0.35	-119.3	4.2	0.75
Class-B	1.48	-116.5	2	0.821

Comparison with the State-of-the-

Index	This work Class-C	This work Class-B	[25] IEEE Transactions on Circuits and Systems II (2019)	[26] IEEE Trans. Very Large Scale Integr. (VLSI) Syst. (2015)	[27] IEEE Journal of Solid-State Circuits (2017)
Technology	130 nm	130 nm	40 nm	180 nm	65nm
VDD(V)	1	1	0.6	0.65	0.8
Fosc (GHz)	2.3-3.07	2.25-3.0	1.57	5.23	7.9
	0.35 QVCO	1.48 QVCO	1.32 QVCO	2.37 VCO	27.2 QVCO
FTR (%)	28.2	28.5	NA	49	NA
	0.77	0.751	NA	NA	NA
PN@ 1MHz	-119.3	-116.5	-118.6	-115.1	-143@ 10MHz
Phase error			NA	NA	
Area(mm2)	0.34	0.34	0.62	0.828	0.34
FoM	-192	-183	-184.4	-185.7	-186.6
FoMT	-201.3	-192.1	NA	-199.5	NA
FoMA	-196.7	-187.7	-186.5	-186.5	NA

Conclusion

- The thesis contributions can be summarized in the following points:
- Proposed class-AB/F PA uses:

1. Reconfigurable off-chip inter-stage and output stage matching networks for 0.1 – 4.2 GHz.
2. Operates in class-AB or class-F, according to the biasing voltage of the driver and the output stages of the PA.
3. Inductorless UWB input matching is implemented with low voltage devices, and the Complementary Current-Reuse common-gate with active shunt feedback is used as input stage to achieve broadband input matching from 0.1 to 5GHz.

- Proposed I/Q De/Modulator uses:

1. Ultra-Wideband (UWB) I/Q demodulator.
2. Reconfigurable wideband I/Q modulator.
3. Reconfigurability of modulator is achieved by high coupling wideband five port transformer and switching capacitors bank.
4. Capacitive Cross Coupling (CCC)common gate configuration is used for both IF stage and RF stage to rise the operation speed of the demodulator and modulator.

Conclusion (cont.)

- Proposed class-C QVCO uses:

1. Series coupling quadrature class-C voltage-controlled power oscillator (S-QVCO).
2. Using high Q-factor switched LC tank circuit to widen the frequency tuning range (FTR) and improve the oscillator phase noise performance.
3. Class-C operation is selected to reduce the power consumption, improve the phase noise, and also increase the FoM.
4. The proposed Class-C QVCO consumes 0.35mW, and has phase noise of -119.3, and FTR of 28.2%. Finally, the core area of the proposed QVCO is 0.34 mm^2.
5. The FoM of Class-C QVCO is increased by 9 dB compared to Class-B QVCO.

Future work

- Implementation and fabrication of all parts for RF transceiver including RF power amplifier, I/Q De/modulator, and QVCO.
- The work done in this thesis would be a core for designing future phased array or MIMO transceivers.
- Proposing a new wideband power amplifier for millimeter wave band with larger output power using power combining techniques.
- Design class-D VCO that has better performance in terms of power efficiency, power consumption and phase noise compared to Class-C VCO.

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Thank you